After Sales Technical Documentation

SERVICE MANUAL

[NMP Part No.0275188]

RAE/RAK–1 SERIES CELLULAR PHONE/ PERSONAL DIGITAL ASSISTANT

NOKIA
MOBILE PHONES

Original 05/97

After Sales Technical Documentation

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
0275188	**08/96**	**RW**	**Original**
	05/97	**RW**	**Update**

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Warnings and Cautions

This manual is intended for use by qualified service personnel only.

Please refer to the phone's user guide for instructions relating to operation, care and maintenance including important safety information. Note also the following:

Warnings:

- **CARE MUST BE TAKEN ON INSTALLATION IN VEHICLES FITTED WITH ELECTRONIC ENGINE MANAGEMENT SYSTEMS AND ANTI–SKID BRAKING SYSTEMS. UNDER CERTAIN FAULT CONDITIONS, EMITTED RF ENERGY CAN AFFECT THEIR OPERATION. IF NECESSARY, CONSULT THE VEHICLE DEALER/MANUFACTURER TO DETERMINE THE IMMUNITY OF VEHICLE ELECTRONIC SYSTEMS TO RF ENERGY.**
- **THE HANDPORTABLE TELEPHONE MUST NOT BE OPERATED IN AREAS LIKELY TO CONTAIN POTENTIALLY EXPLOSIVE ATMOSPHERES EG PETROL STATIONS (SERVICE STATIONS), BLASTING AREAS ETC.**
- **OPERATION OF ANY RADIO TRANSMITTING EQUIPMENT, INCLUDING CELLULAR TELEPHONES, MAY INTERFERE WITH THE FUNCTIONALITY OF INADEQUATELY PROTECTED MEDICAL DEVICES. CONSULT A PHYSICIAN OR THE MANUFACTURER OF THE MEDICAL DEVICE IF YOU HAVE ANY QUESTIONS. OTHER ELECTRONIC EQUIPMENT MAY ALSO BE SUBJECT TO INTERFERENCE.**

Cautions:

- Servicing and alignment must be undertaken by qualified personnel only.
- Ensure all work is carried out at an anti–static workstation and that an anti–static wrist strap is worn.
- Ensure solder, wire, or foreign matter does not enter the telephone as damage may result.
- Use only approved components as specified in the parts list.
- Ensure all components, modules screws and insulators are correctly re–fitted after servicing and alignment. Ensure all cables and wires are repositioned correctly.

Company Policy

Our policy is of continuous development; details of all technical modifications will be included with service bulletins.

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IMPORTANT

While every endeavour has been made to ensure the accuracy of this document, some errors may exist. If any errors are found by the reader, NOKIA MOBILE PHONES Ltd should be notified in writing.

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RAE/RAK–1 SERIES SERVICE MANUAL
OVERALL CONTENTS

Chapter 1

Overview

CONTENTS – Overview

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List of abbreviations

AC	Alternating Current
AFC	Automatic Frequency Correction
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
BB	BaseBand
CMT	Cellular Mobile Telephone
COB	Chip On Board
CODEC	COder/DECoder
CRC	Cyclic Redundancy Check
CTRLU	ConTRoL Unit
DAI	Digital Audio Interface
DBUS	Data BUS (NMP’s internal name)
DC	Direct Current
DSP	Digital Signal Processor
DSPU	Digital Signal Processing Unit
DTMF	Dual Tone Multiple Frequency
DTX	Discontinuous Transmission
EEPROM	Electrically Erasable Read Only Memory
FAX	Facsimile
GSM	Global System for Mobile communications
HF	Hands–Free
HFJ	Hands–Free Junction box
HS	HandSet
HW	HardWare
IC	Integrated Circuit
IF	Intermediate Frequency
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LNA	Low Noise Amplifier
MBUS	Message BUS
MCM	Multi Chip Module
MCU	MicroController Unit

NMI	Non–Maskable Interrupt
NTC	Negative Temperature Coefficient
PC	Personal Computer
PCB	Printed Circuit Board
PCN	Personal Communication Network
PDA	Personal Digital Assistant
PHF	Personal Hands–Free
PIO	Parallel Input/Output
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
PWRU	PoWeR Unit
RAM	Random Access Memory
RBUS	Responder BUS
RF	Radio Frequency
RFI	Radio Frequency Interface
RLP	Radio Link Protocol
ROM	Read Only Memory
RPE–LTP–LPC	Regular Pulse Excitation–Long Term Prediction–Linear Predictive Coding
RX	Receiver
SCL	Small Custom Logic
SIM	Subscriber Identification Module
SIO	Serial Input/Output
SMD	Surface Mount Device
SRAM	Static Random Access Memory
TDMA	Time Division Multiple Access
TX	Transmitter
UHF	Ultra High Frequency (300MHz – 3GHz)
UIF	User InterFace
VAD	Voice Activity Detection
VCXO	Voltage Controlled Crystal (”Xtal”) Oscillator
VHF	Very High Frequency (30 MHz – 300 MHz)

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Introduction

The NOKIA 9000 communicator is a functional *Cellular Mobile Telephone (CMT)* extended to incorporate a *Personal Digital Assistant (PDA).* The unit is of a modular design incorporating the following:

– A CMT providing access to the GSM / PCN networks.

– A PDA providing a User interface that supports personal handsfree audio, graphical high resolution display, control keys and a QWERTY keyboard for text input.

The two parts are combined with a hinge and all data transfer between these two physical modules is performed over an asynchronous, 2–wire, serial bus called RBUS.

Summary of product features

The 9000 provides an extented UI with appropriate new applications and access to both voice and data services over the GSM network. The following table lists the main features on both categories.

Table 1. List of NOKIA 9000 applications

Application	Features
Phone	* call initiating using contact manager app., using call stack, or keypad dialling * speakerphone control, DTMF, multiple calls conference calls, calling/called party ID, call timer counters * settings
FAX	*sending/receiving/forwarding * sending/forwarding based on a new document or an existing one * manual, call stack, or contact manager based recipient selection * viewing tools * settings on fax call divert & cover page
SMS	* sending/receiving * sending based on a new or an existing document * business card exchange via SMS * DTMF service cards * settings
Contact manager	* communication contact data handling * default + user customisable * keeps track of recent communication
Memos	* document editing & viewing * viewer for FAX, WWW (World Wide Web), and JPEG * printing and sending (SMS, FAX, E–mail)
E–mail & VAS Access	* Internet apps using TCP/IP: WWW, Telnet, SMTP/IMAP * VT100 terminal emulator
System	* user profile data applied by SMS business card sending & FAX cover page * security: PIN, lock code, network password, code control, contact manager information visibility control

Table 1. List of NOKIA 9000 applications (continued)

Application	Features
PC connectivity	* AT commands, PC backup, new app. installation, document & file transfer, contact manager contents exchange in ASCII
Calendar	* month/day view, link to notes possible, to–do lists, event based alarms
Extras	* basic calculator * world time clock * ringing tone composer * other small applications loaded from PC

Table 2. Basic GSM services

Group	Feature	Rate (bits/s)	Notes
GSM Speech		13 k	Full rate
GSM Data	Non–transparent	9.6k, 4.8k, 2.4k	Full rate
GSM Teleservices	Facsimile (Grp 3), SMS, Cell Broadcast		Cell broadcast, transparent fax
GSM Supplementary Services	Selected sub–set		

Table 3. Other communication protocols/formats supported

Application	Protocol	Notes
Email	SMTP, IMAP4, MIME1	
All Internet apps	TCP/IP	
WWW	HTTP 1.0, HTML 2.0	JPEG, GIF
Terminal	VT100	
PC Connectivity	RS232, IrDA	
Module interconnection	RBUS	
Ext. serial i/f	MBUS	

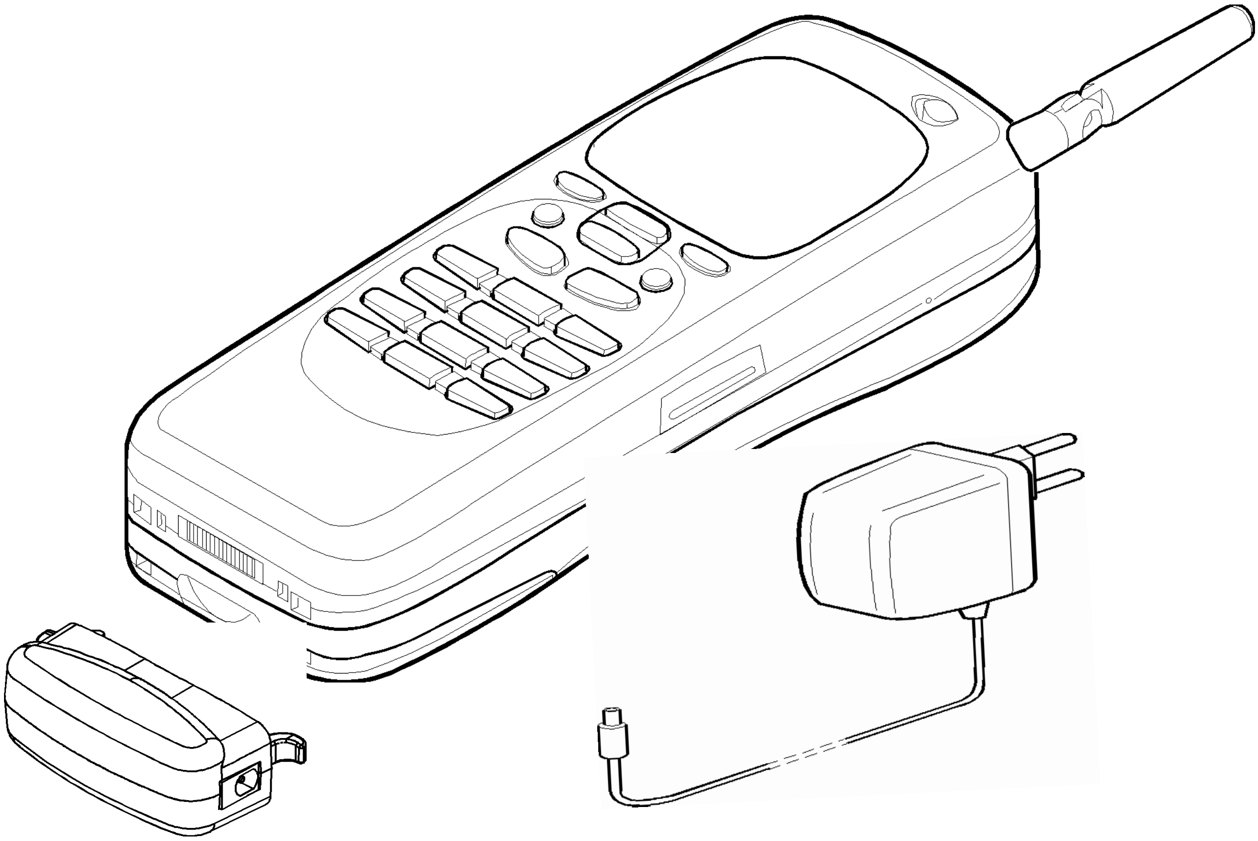

Figure 1. Basic Kit

The NOKIA 9000 communicator integrates the functionality of the Nokia DTP–2 GSM/PCN data adapter card on its modified baseband and adds a second, improved user interface for data applications such as fax, terminal emulator, and graphical Internet browsers, e.g., World Wide Web (WWW).

The transceiver utilises common core electronics (DCT2) which can be easily modified to comply with all digital standards in the world. The HD841 is a GSM / PCN project to develop a series of products for the GSM PCN markets and the 9000's RF block is of this DCT2 generation. The baseband section and accessories are derived from the DCT1 generation (HD740, HD745).

Figure 2. Personal Digital Assistant

GSM/PCN Networks

GSM is originally a pan–European digital cellular network standard, later phrased as the Global System for Mobile Communications. The standard is defined jointly by all related parties in the European Telecommunication Standard Institute (ETSI).

PCN is a European cellular mobile telephone standard based on the GSM/DCS–1800 standard also defined by the ETSI. The current PCN network licences have been granted to operators in Germany and the UK.

Modular Structure

The transceiver consists of the following modules:

GE8/GE9 – Transceiver modules for PCN and GSM
GP1 – Personal Digital Assistant module
GK2 – Combined User interface module (CMT/PDA)
GEM1 – SIM and audio module (CMT)

In addition, the CMT baseband contains multichip modules (MCM) that are in fact submodules but should be considered as components for the CMT unit.

The LCD module(GK2) consists of a CMT U/I module and a graphic LCD module for the PDA. GK2 contains an insert for an antenna; this Antenna is by default a helix with a joint but can be replaced with a whip type.

The CMT and PDA modules are assembled inside the same covers and connected via a board to board connector. The LCD module and antenna are installed in the lid part which is in turn connected to the main part with a hinge; the LCD module being connected to the PDA module through the hinge with a flexible flat cable. The antenna is connected to the CMT module via coax cable.

The SIM flex module contains the SIM card holder, the buzzer, and the standard handset acoustic components, i.e., microphone and earpiece, on a flex carrier. Handsfree audio components, i.e., microphone and speaker, are assembled in cavities in a magnesium chassis and connected on the PDA via a pair of cables.

In addition the NOKIA 9000 has a dedicated attachable Li Ion battery and contains 2 cells with 730 mAh capacity (1Q/96) plus necessary protection circuitry with external connector.

The CMT module is covered by EMC/EMI shields, i.e., magnesium chassis and metallized plastic shield, of which the chassis is also extended to cover critical parts of the PDA module, e.g., switched mode power supply (SMPS) and infra–red (IR) transceiver circuit. A simplified functional diagram of the modular structure is illustrated below. The figure also includes the unit’s external interfaces.

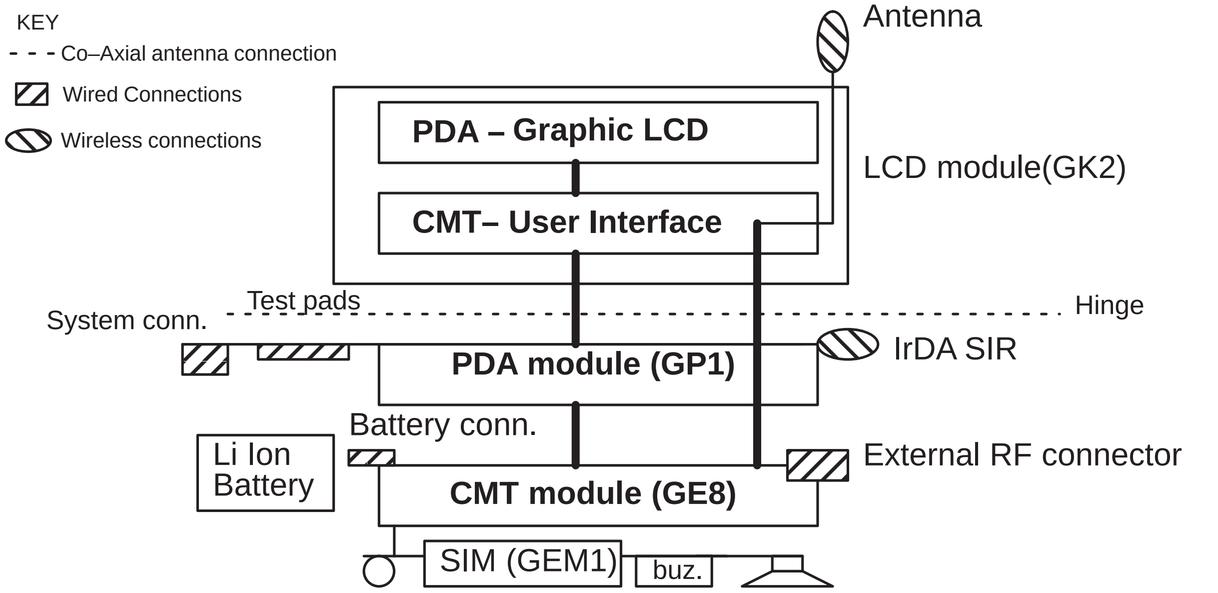

Figure 3. Modular Structure

Product Variants

The NOKIA 9000 communicator has the type designator RAE/RAK–1N where RAE refers to the GSM version and RAK ,the PCN version. The table below shows the variants that apply to this product; these variations only affecting the QWERTY keymat layouts, illustrated in Figure 4 overleaf.

Table 4. NOKIA 9000 communicator Product Variants

Type Designation	Language Version
RAE/RAK–1NA	UK English
RAE/RAK–1NB	German
RAE/RAK–1NC	French
RAE/RAK–1NE	Scandinavian

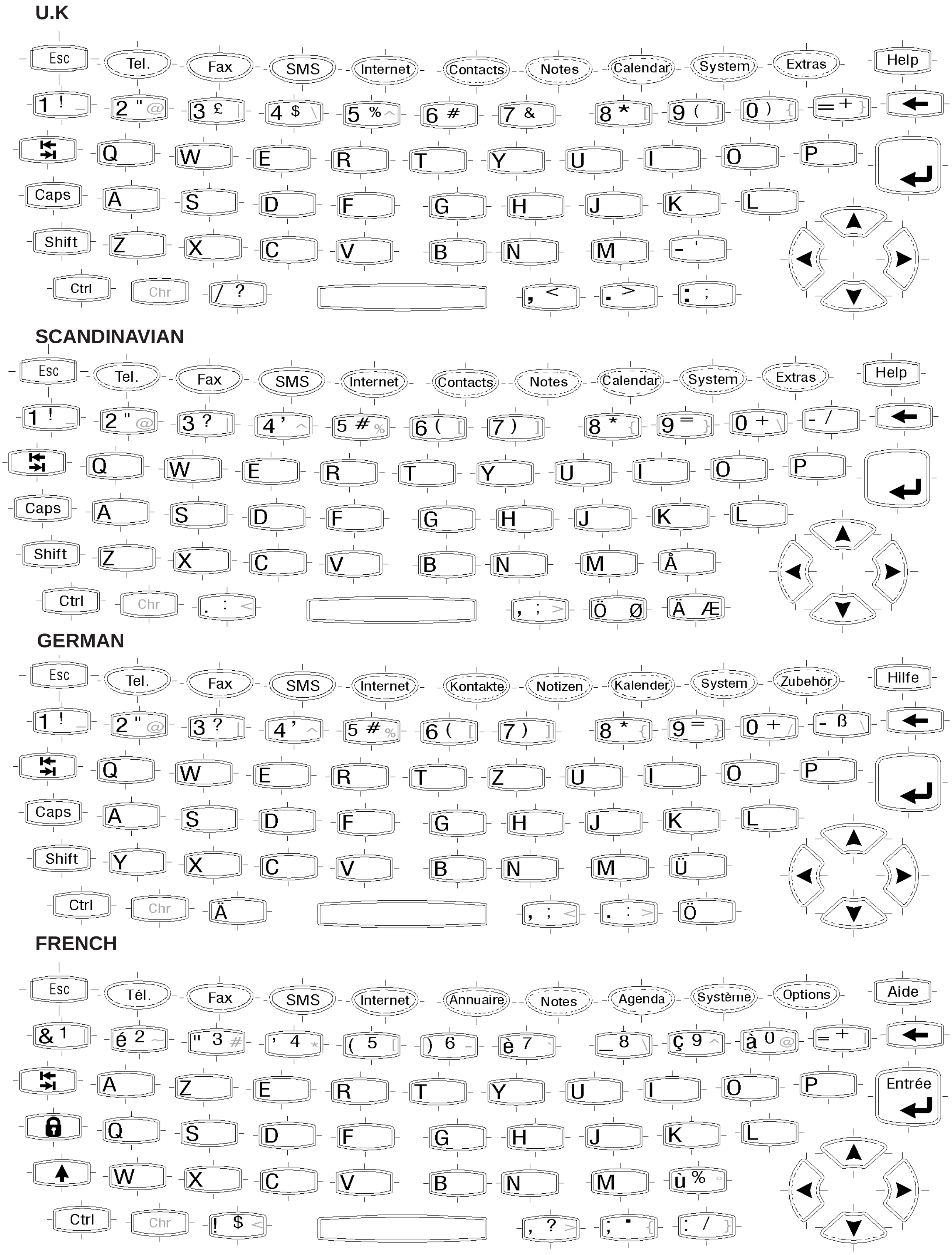

Figure 4. PDA QWERTY keypads

Sales Packages

The NOKIA 9000 product family is a first generation GSM / PCN handportable. The family contains a basic sales package for portable use and optional accessories for office and mobile use. There is only one Nokia design version of the transceiver. However, product variation is done by changing the QWERTY keymat according to the target country.

The basic sales package consists of the following products:

- NOKIA 9000 communicator transceiver (RAE–1Nx/RAK–1Nx)
- Standard Battery Pack (BLK–4S)
- Fast Travel Charger (ACH–3)
- Power Adapter Module (PAR–1)
- PC Diskette (connection software – Windows)
- User's Manual & Quick Guide
- Packaging materials
- Security Code Envelope

Accessories

The following tables outline accessory part numbers and specifications:

Table 5. Batteries

Name of battery	Type code	Material code	Notes
Battery	BLK–4S	0670153	730 mAh Li–Ion

Table 6. Chargers

Name of charger	Type code	Material code	Notes
Fast Travel Charger	ACH–4E	0675008	Euro Mains voltage 200...240 V
Fast Travel Charger	ACH–4X	0675009	UK Mains voltage 200...240 V
Fast Travel Charger	ACH–4A	0675036	Australian Mains voltage 200...240 V
Fast Travel Charger	ACH–4P	0675065	Philippines Mains voltage 200...240 V

Table 7. HF Car Installation

Name of accessory	Type code	Material code	Notes
HF Junction Box	HFJ–3	0694009	
Hands Free Speaker	HFS–6	0692005	
Hands Free Microphone	HFM–10	0690009	

Table 7. HF Car Installation

Name of accessory	Type code	Material code	Notes
Power Cable	PCH–4	0730009	
External Audio Handset	HSU–1	0640047	
Swivel Kit	MKR–1	0620033	
Mounting Plate	MKE–1	0650007	
Installation Guide, HF Car kit	CARK 60	9385069	

Table 8. Data and office accessories

Name of accessory	Type code	Material code	Notes
RS232 cable	DLR–1	0730077	
Spare battery charger	DCH–4	0675107	To be used with ACH–4x

Technical Summary

The transceiver electronics consist of the following modules:

– PDA (PIM & extended UI control),
– Radio System (RF + System blocks),
– UIF
– SIM and audio submodule.

The UIF Module is connected to the PDA module with a flex cable and a connector. The PDA module is connected to the Radio System Module using a 44 pin board–to–board connector.

The System block (Baseband and RF modules) are interconnected with PCB wiring and the transceiver is connected to accessories via a bottom system connector plus an RF connector in the other end of the device. An IR eye for wireless data exchange locates to the same end as the external RF connector.

The PDA module provides the hardware platform for the extended UI with an integrated CPU and peripheral control IC (E3G), memories (DRAM, Flash), power circuitry (SMPS), IR electronics and external RS buffering.

The PDA power supply generates power for;
– Graphical LCD (22V)
– Basic PDA logic (3.3 V)
– Flash programming (dynamic) (5V)

The System block contains the MCU and DSP environments, System BB IC (D2CA), memories, audio processing and RF interface hardware (RFI). On board power supply circuitry delivers operating voltages for both System and RF blocks.

The general purpose microcontroller, Hitachi H8, communicates with the DSP, memories and Logic control IC (D2CA) with an 8–bit data bus.

The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station.

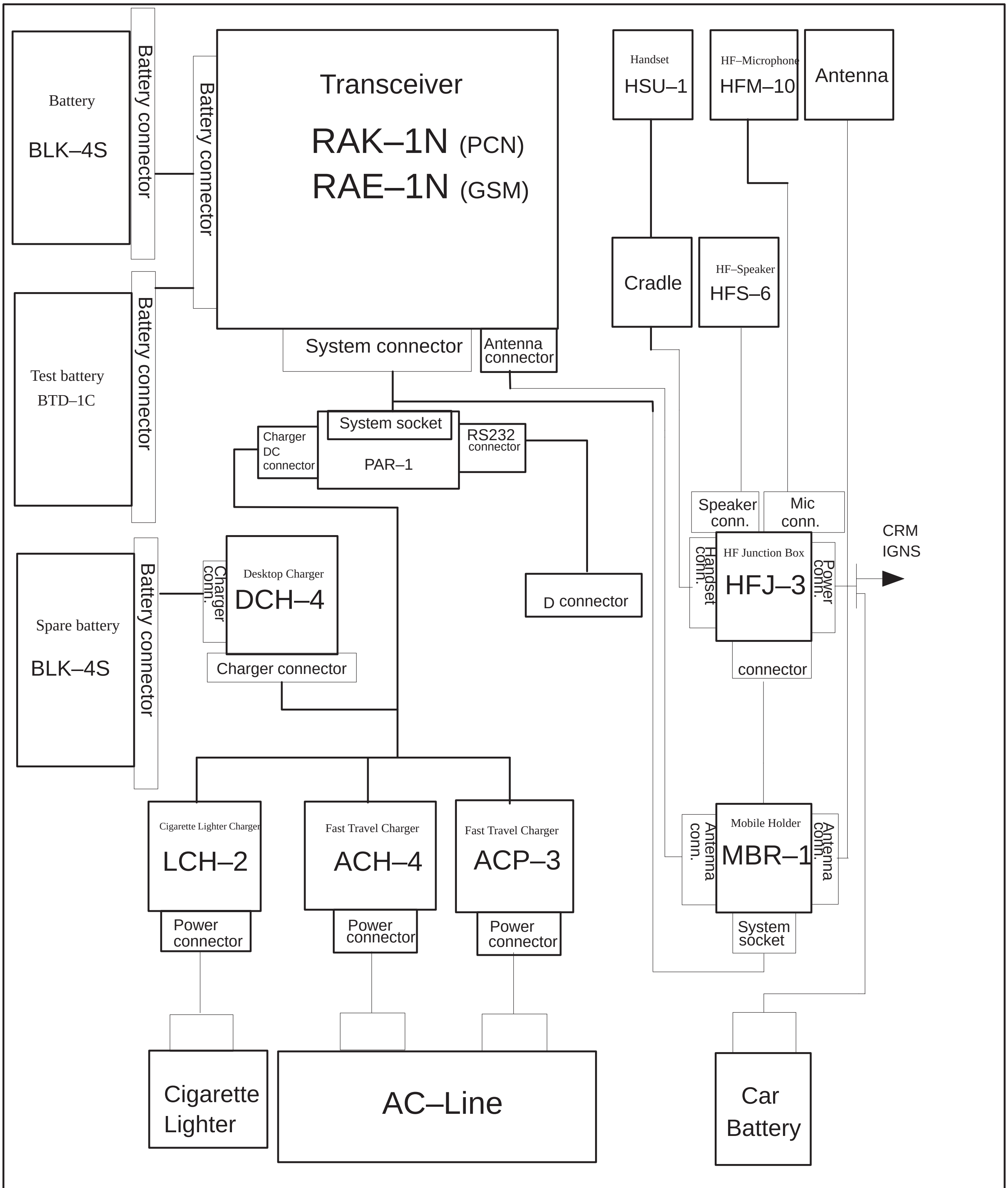

Figure 5. Interconnection Diagram

Mechanical Characteristics

Table 9. Mechanical Characteristics

RAE–1	Dimensions (WxLxH) / mm	Weight / g	Volume/ cm^3	Notes
Transceiver with standard battery pack	65*176*39	397	400	If antenna is included, length is 189
Transceiver w/o battery pack	same	315	300	
Radio module (inc. chassis + shield)	57*170*16	73	–	
UIF module	57*170*11	87	–	
Mechanics		155	–	
Battery pack BLK–4S	52*61*19	83		

Environmental Conditions

Temperature Conditions

Table 10. Allowed Ambient Temperatures

Environmental condition	Ambient temperature (degrees Celcius)	Notes
Normal operation conditions	+15°C...+35°C	Office environment
Extreme operation conditions	–20°C...+55°C	GSM Specifications fullfilled
Reduced performance conditions	–30°C...–20°C	Operation possible after warm–up, LCD's might operate slowly or cessate operating.
	+55°C...+65°C	Connection can be established
	+65°C...+75°C	Operational only for a short period
Intermittent operation condidions	–40°C... –30°C	Operation not possible but attempt to operate will not damage the device
	+75°C ...+85°C	
Cessation of operation	< –40°C or > +85°C	No storage or operation possible without permanent damage
Storage conditions	–40°C ... +70°C	
Charging	0°C ... +45°C	Li–Ion charging recommendation by the vendor; exceeding these limits will result in reduced capacity and longer charging times

Vibration and Free Fall

The transceiver meets the module phase error requirements which equates to a total RMS vibration in the range 10 Hz to 150 Hz of 0.5 g. The transceiver has been drop tested to withstand an 80cm drop onto a solid floor.

Humidity and Water Resistance

Relative humidity range in normal operation conditions : 20 ... 75 %.

Relative humidity range allowed : 5 ... 95 %

The transceiver is not waterproof and care should be taken if used in damp conditions.

Maximum Ratings

Table 11. Maximum Ratings

Pin / Conn	Line Symbol	Minimum	Typical / Nominal	Maxi-mum	Unit / Notes
1 / Battery	VBATT	5.0	7.2	9.0	V / Phone off in min . extreme, PDA on
1 / 3 / Char	VCHAR	10.0	12.0	13.0	V (unloaded)

Operating Instructions

Operating instructions are given in the QUICK GUIDE in the Appendix of this manual and the USER'S GUIDE that comes with the product. The transceiver is provided with a HELP system via both keypads (lid open/closed). Also, 'on line' help will be available on the Internet via the Nokia–club service.

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Chapter 2

–Transceiver GE8/GE9–
Baseband Block

CONTENTS –Baseband

List of Figures

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Introduction

The baseband engine consists of two multi chip modules (MCM) mounted along with other baseband circuitry and RF parts on a single multilayer PCB. The chassis of the radio unit has separating walls between baseband and RF. All components are surface mounted. Transceiver GE8 is GSM; Tranceiver GE9 is PCN

The connection to the NOKIA 9000 communicator PDA module is made using a board to board connector. The connections to the User Interface module (UIF) are made through the 'passive' PDA module. Besides the PDA board to board connector only the SIM/audio and battery connector are on the baseband module. There is no physical connector between the RF and baseband sections.

Technical Summary

Because of extreme size constraints on this product new production technology will be used. Most of the baseband ICs will be integrated in two multi chip modules. These MCMs and all other baseband circuits are mounted on a single multilayer printed circuit board. This board contains also RF parts. The chassis of the radio unit has separating walls between baseband and RF. All components of the baseband section including the MCMs are surface mountable. They are soldered using reflow. The connection to Responder PDA module is made using a board to board connector. The connections to the User Interface module (UIF) are made through the PDA module. Besides the PDA board to board connector only the SIM/audio connector and battery connector are on the baseband module. There is no physical connector between the RF and baseband sections.

Table 1. List of Functional Submodules

Name of submodule	Function
CTRLU	Control Unit for phone
PWRU	Power supply and charging electronics
DSPU	Digital Signal Processing block
AUDIO	Analog audio processing and PCM encoding/decoding
ASIC	D2CA GSM/PCN system specific ASIC; several functions
RFI	RF – baseband interface (analog signals)

The above blocks are only functional blocks and therefore have no type or material codes. Physically the baseband contains two submodules, MCM1 and MCM2 which utilise COB (chip on board) packaging technology. The MCM 1 contains the 7 ICs in the CTRLU submodule plus bypass capacitors and some resistors.

The MCM 2 contains the 6 ICs in DSPU, AUDIO, ASIC and RFI submodules plus bypass capacitors and some resistors. The PWRU module is laid out in the CMT board using conventional SMD assembly. The rest of the functional modules are partly packaged in the MCM's and partly SMD assembled on the CMT board. In the latter description of the modules the functional partitioning will be used.

Table 2. List of Physical Submodules

Name of submodule	Function
MCM1	Contains MCU, SCL, 2xFLASH, 2xSRAM and EEPROM
MCM2	Contains DSP, 2xSRAM, ASIC, RFI and CODEC

Interconnection Diagram

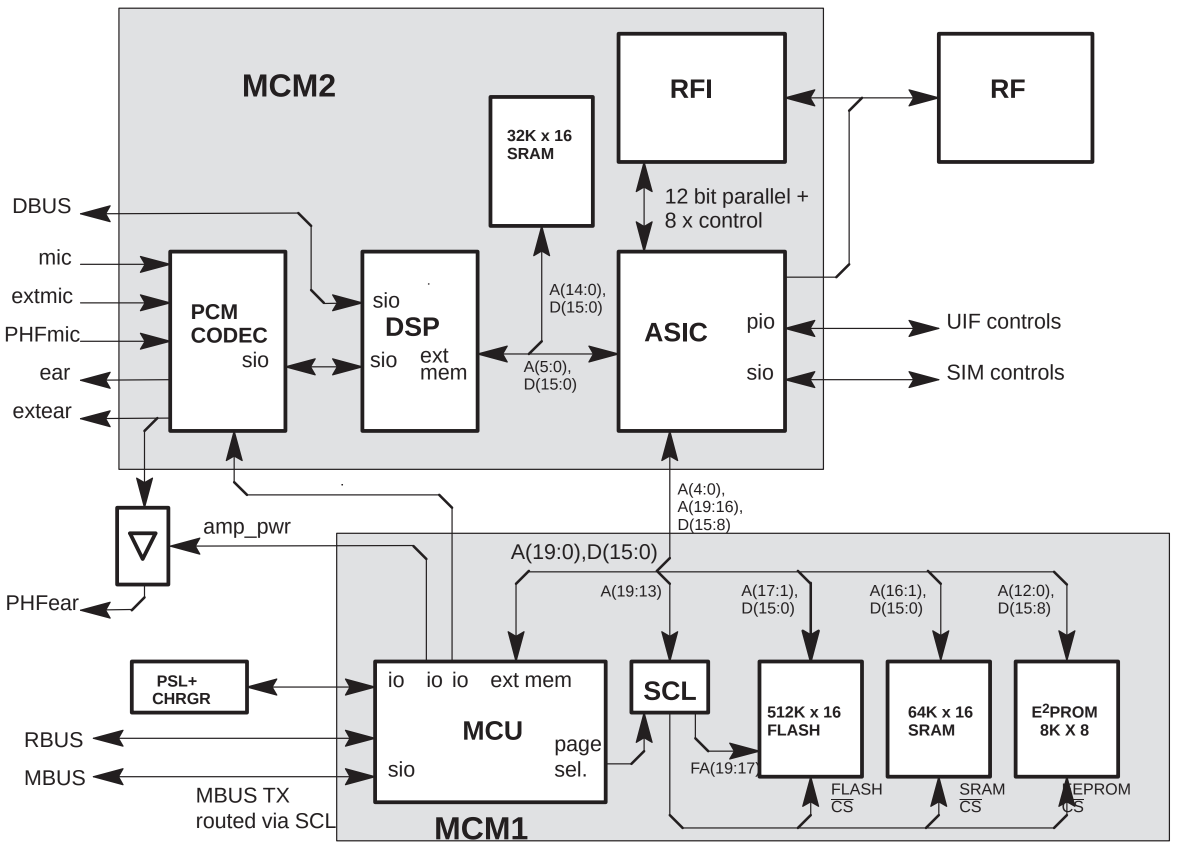

Figure 1. Interconnection diagram

Modes of Operation

There are four different operation modes

- active mode
- idle mode
- acting dead mode
- power off mode

Active Mode

In the active state all circuits are powered and part of the module may be in idle mode.

Idle Mode

The module is usually in the idle mode when there is no call and the phone is in SERV. In the idle mode circuits are reset, powered down and clocks are stopped or the frequency reduced. All the clocks except the main clock from VCXO can be stopped in that mode. Whether the SIM clock is stopped or not depends on the network.

Acting Dead Mode

The acting dead mode means that the baseband is powered but there is no difference from the power off mode from the user point of view. The acting dead mode is used for performing some necessary control functions such as battery voltage measurement and reporting to PDA module.

Power Off Mode

In power off mode only the circuits needed for power up are powered. This means that only power up block inside the PSL+ is powered. The power key is pulled up with a pull up resistor inside the PSL+.

Performance Specifications

DC Characteristics

Table 3. Supply Voltages and Power Consumption

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
4 / BATT 1 / B2B 44 / B2B 1 / SIMFLEX	VBATT, VB	5.75V	7.2V	–	Software limit
		4.8V	7.2V	8.7 +/–0.3V	Hardware limits (cut–off min, charging max)
		4.8V	7.2V	7.6 +/–0.3V	Hardware limits during a call

Table 3. Supply Voltages and Power Consumption (continued)

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
14 / B2B 31 / B2B	VCHAR	10.0V	12.0	13.0V	Charger specifications, without load
	VA1	4.5V	4.65V	4.8V	Imax = 40mA
	VA2	4.5V	4.65V	4.8V	Imax = 80mA
	VA3	4.5V	4.65V	4.8V	Imax = 200mA
11 / B2B	VL1	4.7V	4.85V	5.0V	Imax = 150mA
	VL2	4.7V	4.85V	5.0V	Imax = 150mA
	VREF	4.55V	4.65V	4.75V	Imax = 5mA
16 / B2B	VF	11.4V	12V	12.6V	Flash programming voltage

Table 4. Digital control signals

6 / B2B	BACKLIGHT	0V		0.7V	Output low, backlights off	Display and keyboard illumination control
		4.7V	4.85V	5.0V	Output high, backlights on	
8 / B2B	RBUSRXD	3.6V	4.85V	5.0V	State ”1”	RBUS received data to CMT
		0V	0.2V	0.7V	State ”0”	
9 / B2B	RBUSTXD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS transmitted data from CMT
		0V	0.2V	0.7V	State ”0”	
12 / B2B	XPWRON	0V	0V	0.7V	Input low, power on/off	
			4.65V		Floating when inactive. A pull–up in PSL+.	
15 / B2B	BUZPWR	0V		0.7V	Input low, buzzer on	
		5.3V	7.2V	8.4V	Input high, buzzer off	
20 / B2B 19 / B2B 18 / B2B 17 / B2B	COL(3:0)	0V		0.7V	Output low	keyboard columns
		4.7V	4.85V	5.0V	Output high	

27 / B2B 26 / B2B 25 / B2B 24 / B2B	UIF(3:0)	0V		0.7V	Output/Input low	keyboard row lines/ display data lines
		4.7V	4.85V	5.0V	Output/Input high	
28 / B2B	UIF4	0V		0.7V	Output/Input low	keyboard row read/write strobe for LCD driv-er
		4.7V	4.85V	5.0V	Output/Input high	
29 / B2B	UIF5	0V		0.7V	Output/Input low	keyboard row LCD driv-er register select
		4.7V	4.85V	5.0V	Output/Input high	
30 / B2B	UIF6	0V		0.7V	Output/Input low	enable strobe for LCD driv-er
		4.7V	4.85V	5.0V	Output/Input high	
32 / B2B	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
33 / B2B	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
34 / B2B	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS re-ceived data to CMT
		0V	0.2V	0.7V	State ”0”	
35 / B2B	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS trans-mitted data from CMT
		0V	0.2V	0.7V	State ”0”	
36 / B2B	M2BUS	0V		0.7V	Input low level	Isink<5m ABaud rate 9600 bits/s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
38 / B2B	LID	3.3V		4.9V	Lid open	Cover switch status
		0.0V		1.0V	Lid closed	
2 / SIMFLEX	BUZZER	0V		0.7V	Output low, buzzer on	Buzzer on SIM flex
		5.3V	7.2V	8.4V	Output high, buzzer off	

6 / SIMFLEX	SIMCLK	3.6V	4.85V	5.0V	State ”1”	Clock for SIM card
		0V	0.2V	0.7V	State ”0”	
7 / SIMFLEX	SIMRESET	4.7V	4.85V	5.0V	Output high	Reset for SIM card
		0V		0.7V	Output low	
8 / SIMFLEX	VSIM	4.7V	4.85V	5.0V		SIM card reader supply voltage
9 / SIMFLEX	SIMDATA	0V		0.8V	Input low level	Data for SIM card
		2.0V		5.0V	Input high level	
		0V	0.2V	0.7V	Output low level	
		4.7V	4.85V	5.0V	Output high level	

Table 5. Battery monitoring signals

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maxi-mum	Unit / Notes
11 / SIMFLEX 12 / SIMFLEX	MICN MICP		5 mV_{rms}	19 mV_{rms}	Differential
3 / SIMFLEX 4 / SIMFLEX	EARN EARP		124 mV_{rms}	1.965 V_{rms}	Differential, $R_L = 32\Omega$
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
1 / PHF 2 / PHF	PHFEARP PHFEARN		1.0 V_{rms}	2.8 V_{rms}	Differential $R_L = 8\ \Omega$
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	minimum DC–level 2.0V.
42 / B2B	EXTEAR		160 mV_{rms}	410 mV_{rms}	minimum DC–level 2.0V.

AC Characteristics

Table 6. Audio Signals

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
11 / SIM-FLEX 12 / SIM-FLEX	MICN MICP		5 mV_{rms}	19 mV_{rms}	Differential
3 / SIMFLEX 4 / SIMFLEX	EARN EARP		124 mV_{rms}	1.965 V_{rms}	Differential, $R_L = 32\Omega$
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
1 / PHF 2 / PHF	PHFEARP PHFEARN		1.0 V_{rms}	2.8 V_{rms}	Differential $R_L = 8\ \Omega$
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	minimum DC–level 2.0V.
42 / B2B	EXTEAR		160 mV_{rms}	410 mV_{rms}	minimum DC–level 2.0V.

Table 7. Handportable audios, microphone

HPMIC 1kHz rms		NOTES
MRP pressure	+3 dBPa	5 cm from MIC
MIC pressure	–2 dBPa	about 5 dB attenuation
MIC output	5.0 mV	mic sensitivity –64 dB (6.3 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Codec gain	29 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–11 dBmO / 140 mVrms	0 dBmO = 490 mV

Table 8. Handportable earpiece

HPEAR 1 kHz rms		NOTES
Level	–6.0 dBmO / 980 mVrms	0 dBmO = 1965 mVrms
Codec gain	–18 dB nominal –8 dB max. volume	18 dB atten. Controllable 0...–30 dB. Maximum volume +10 dB
Codec output	120 mVrms nominal 390 mVrms max.volume	
Earpiece pressure	+6 dBPa nominal +16 dBPa max. volume	Earpiece impedance 32Ω + 20Ω series resistance in CMT.

Table 9. Personal HF microphone

PHFMIC 1kHz rms		NOTES
MRP pressure	+14 dBPa	50 cm from MIC
MIC pressure	–6 dBPa	about 20 dB attenuation
MIC output	3.1 mVrms	mic sensitivity –64 dB (6.3 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Codec gain	30.5 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–13.5 dBmO / 105 mVrms	0 dBmO = 490 mVrms

Table 10. Personal HF speaker

PHFEAR 1 kHz rms		NOTES
Level	–6.0 dBm0 / 980 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–14 dB nominal –6 dB max. volume	14 dB attenuation. Controllable 0...–30 dB. Maximum volume +8 dB
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Codec output	100 mVrms nominal 245 mVrms maximum	
Booster gain	18 dB	
Speaker input	0.78 Vrms nominal 1.95 Vrms maximum	80 mW average / 8Ω / Bridge tied load. 480 mW average / 8Ω / Bridge tied load.
Pressure	–19 dBPa nominal –11 dBPa maximum	50 cm from speaker. Speaker sensitivity 80 dB/W/1m (Foster T028S21). 0dB = –94 dBPa (20 μPa)

Table 11. Accessory HS microphone

HSMIC 1kHz rms		NOTES
MRP pressure	+3 dBPa	5 cm from MIC
MIC pressure	–2 dBPa	about 5 dB attenuation
MIC output	6.3 mVrms	mic sensitivity –62 dB (7.9 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Handset gain	27 dB	Flat mic response
Accessory level	140 mVrms	
HFJ gain	0 dB	
Cable level	140 mVrms	
Attenuation on system board	21 dB	

Table 11. Accessory HS microphone (continued)

HSMIC 1kHz rms		NOTES
Codec input level	12.5 mVrms	
Codec gain	26 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–6 dBm0 / 250 mVrms	0 dBm0 = 490 mVrms

Table 12. Accessory HS earpiece

HSEAR 1 kHz rms		NOTES
Level	–6.0 dBm0 / 980 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–6 dB	With maximum gain
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Cable level	245 mVrms	min. impedance 1 kΩ
HFJ gain	0 dB	
Accessory level	245 mVrms	
Handset gain	1 dB minimum 18 dB maximum	Hanset gain (–5...+12) dB + 6 dB from single–side to differential conversion
EAR amp. output	310 mVrms minimum 1.95 Vrms maximum	Measured differentially
Earpiece pressure	+1 dBPa minimum +18 dBPa maximum	

Table 13. Accessory HF microphone

HFMIC 1 kHz rms		NOTES
MRP	+15 dBPa	50 cm from MIC
MIC	–5 dBPa	about 20 dB atten.
MIC output when HFJ connected	2.0 mVrms	MIC sensitivity –65 dB (5.6 mV/Pa) (mic output level 3.3 mV without load)
HFJ gain	40 dB	
Cable level	200 mVrms	
Attenuation on system board	21 dB	
Codec input level	18 mVrms	
Codec gain	23 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–6 dBm0 / 250 mVrms	0 dBm0 = 490 mVrms

Table 14. Accessory HF speaker

HFEAR 1 kHz rms		NOTES
Level	–10 dBm0 / 620 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–16 dB nominal	
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Cable level	50 mVrms nominal	minimum impedance 1kΩ
HFJ gain	27 dB	
HFJ output level	1.1 Vrms nominal	
Pressure	about –2 dBPa	50 cm from loudspeaker

Connectors

Connectors to other modules of the product

Table 15. PDA board to board connector (B2B)

Signal Name	Pin(s)	Notes
VB	1,44	Battery voltage to the PDA module.
GND	2,5,7,10,13,21, 22,23,37,39,40	Ground
PHFMICN	3	PHF microphone (negative node)
PHFMICP	4	PHF microphone (positive node)
BACKLIGHT	6	Backlights on/off
RBUSRXD	8	RBUS receive data
RBUSTXD	9	RBUS transmit data
VL1	11	Logic supply voltage (4.7–5.0V)
XPWRON	12	Power key (active low)
VCHAR	14,31	Battery charging voltage.
BUZPWR	15	PWM signal buzzer control input from PDA module
VF	16	Programming voltage for flash.
COL(3:0)	20,19,18,17	Lines for keyboard write
UIF(3:0)	27,26,25,24	Lines for keyboard read and LCD–controller data
UIF4	28	Line for keyboard read and LCD–controller read/write strobe
UIF5	29	Line for keyboard read and LCD–controller data/instruction register selection
UIF6	30	LCD–controller enable strobe
DCLK	32	DBUS–data clock
DSYNC	33	DBUS–data bit sync clock

Table 15. **PDA board to board connector (B2B) (continued)**

Signal Name	Pin(s)	Notes
RDA	34	DBUS received data from the accessories
TDA	35	Transmitted DBUS–data to the accessories
M2BUS	36	Serial bidirectional data and control between the CMT and accessories.
LID	38	Cover switch state from PDA to CMT
EXTMIC	41	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
EXTEAR	42	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
AGND	43	Analog ground for accessories. Connected directly to digital ground on the PCB.

Table 16. **PHF speaker connector**

Signal Name	Pin(s)	Notes
PHFEARN	1	PHF speaker, negative node
PHFEARP	2	PHF speaker, positive node

Table 17. **SIMFLEX Connector**

Signal Name	Pin	Notes
VBATT	1	Battery voltage for buzzer
BUZZER	2	Excitation for buzzer (pull–down)
EARN	3	Differential audio for the earpiece
EARP	4	
GND	5,10	Ground
SIMCLK	6	Clock for SIM data
SIMRESET	7	Reset for SIM
VSIM	8	SIM voltage supply
SIMDATA	9	Serial data for SIM
MICN	11	Differential audio from the microphone
MICP	12	

Connectors out of Transceiver Unit

Table 18. Battery connector

Signal Name	Pin	Notes
BGND	1	Battery ground
TBAT	2	Battery temperature
BTYPE	3	Battery type
VB	4	Battery voltage

Internal Signals and Connections

Table 19. Signals Between RF and D2CA ASIC (MCM2)

Signal Name	Function	Notes
SCLK	Synthesizer clock	From ASIC to RF
SDATA	Synthesizer data	From ASIC to RF
SENA1	UHF and VHF PLL enable	From ASIC to RF
RXPWR	RX supply voltage ON/OFF	From ASIC to RF
SYNTHPWR	Supply voltage ON/OFF	From ASIC to RF
TXPWR	TX supply voltage ON/OFF	From ASIC to RF
TXP	Transmitter power control enable	From ASIC to RF
RFC	26 MHz clock from RF to baseband	From RF to ASIC

Table 20. Signals Between RF and RFI (MCM2)

Signal Name	Function	Notes
AFC	Automatic frequency control voltage	From RFI to RF
TXC	TX transmit power control voltage and RX automatic gain control voltage	From RFI to RF
TXQP,TXQN	differential TX quadrature signal	From RFI to RF
TXIP,TXIN	differential TX in–phase signal	From RFI to RF
PDATA0	LNA gain control	From RFI to RF
RXQ	RX quadrature signal (13 MHz)	From RF to RFI
RXI	RX inphase signal (13 MHz)	From RF to RFI
RFIREF	4.096 V reference voltage	From RFI to RF

Table 21. Signals Between RF and CTRLU (MCM1)

Signal Name	Function	Notes
TRF	RF temperature sensor	From RF to CTRLU

Table 22. Signals Between RF and PWRU

Signal Name	Function	Notes
VREF	Supply voltage for VCXO	From PWRU to RF
VBATT	Battery voltage	From PWRU to RF
GND	Ground	Common ground

Circuit Descriptions

Power Distribution

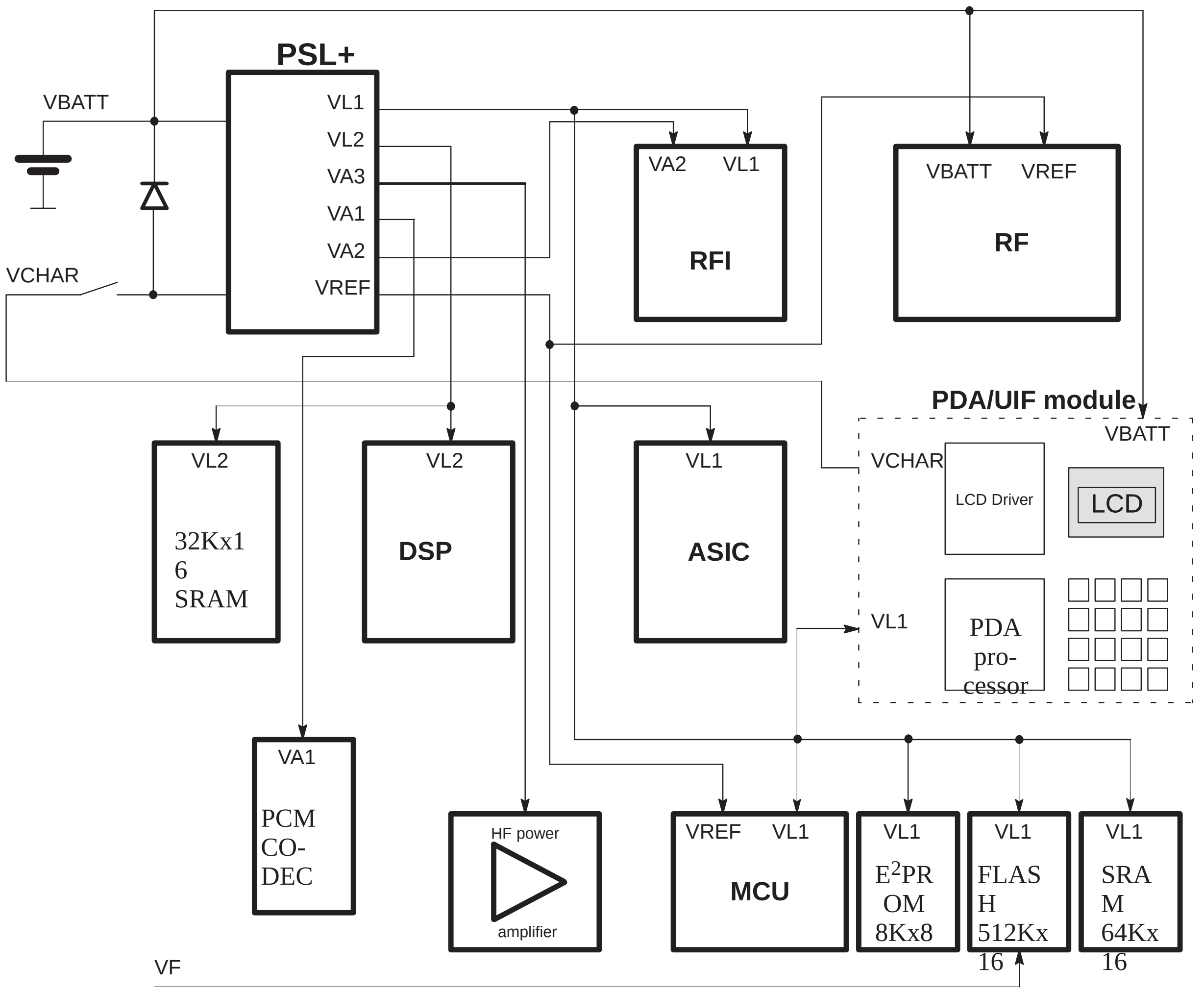

Figure 2. Power Distribution Diagram

Clocking scheme

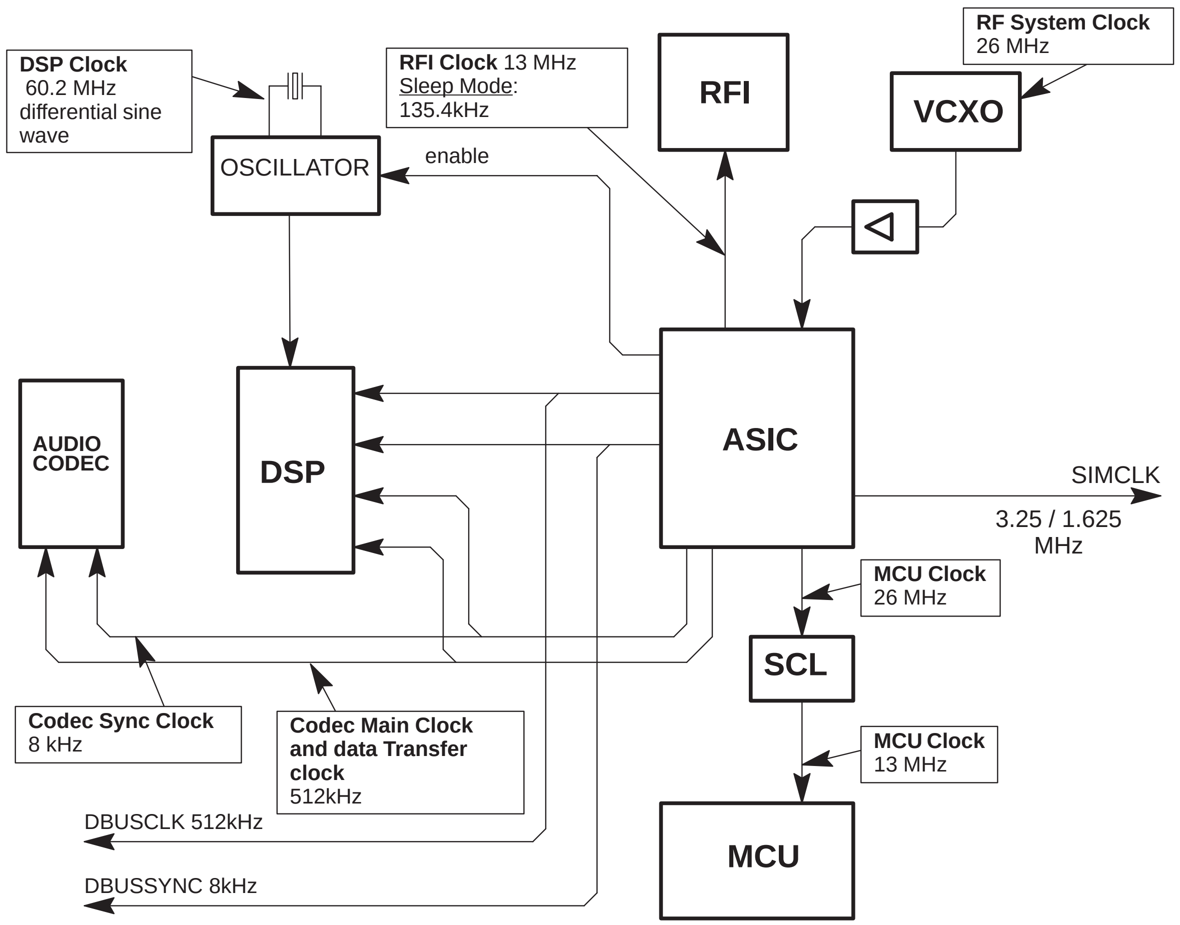

Figure 3. Clocking Scheme

Most of the clocks are generated from the 26 MHz VCXO frequency by the ASIC:

– *26 MHz clock for the MCU*. SCL divides this by two and supplies a 13 MHz clock to the MCU.
– *13 MHz for the RFI.* The ASIC also generates 135.4 kHz sleep mode clock for the RFI.
– *3.25 MHz clock for SIM*. When there is no data transfer between the SIM card and the baseband the clock can be reduced to 1.625 MHz. Some SIM cards also allows the clock to be stopped in that mode.
– *512 kHz main clock for the codec* and for the data transfer between the DSP and the codec.
– *8 kHz synchronisation clock for data transfer* between the DSP and the codec.
– *512 kHz clock and 8 kHz sync. clock for the DBUS data transfer*

The DSP has its own crystal oscillator which can be turned off and on by the ASIC. The DSP uses differential sinusoidal clock. The frequency is 60.2 MHz.

The MCU generates 8 kHz clock to the codec for the control data transfer.

In the idle mode all the clocks can be stopped except 26 MHz main clock coming from the VCXO.

Reset and power control

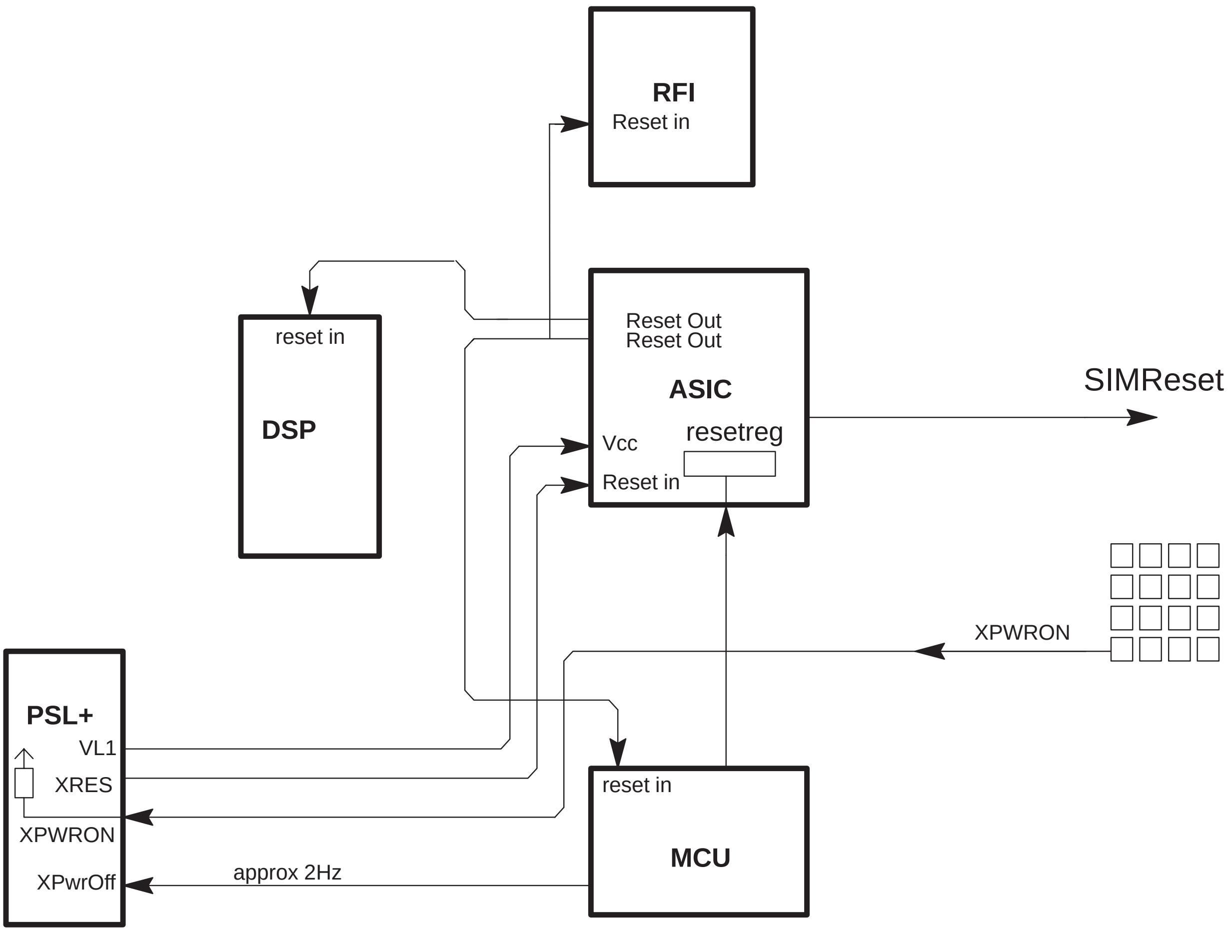

Figure 4.   Reset and Power Control

There are three different ways to switch power on:

Pulling the XPWRON line down e.g by pressing the power key. The PSL+ detects that and switches the power on.

Charger detection on PSL+ detects that charger is connected and switches power on

PSL+ will switch power on when the battery is connected. After that the MCU will detect if power key is pressed or charger connected. If not the power will be switched off

All devices are powered up at the same time by the PSL+. It supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. After about 100 ms the PSL+ releases the reset to ASIC.

ASIC releases the resets to MCU and RFI after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13MHz clock cycles. In our case it is 255. SIM reset release time is according to GSM SIM specifications.

To turn off power for the phone, the user presses the PWR key. The MCU detects this. The MCU cuts off any ongoing call, exits all tasks, acts inoperative to the user and leaves the PSL+ watchdog without resets. After power–down delay, the PSL+ cuts off the supply from all circuitry.

In the acting dead state the phone looks to the user like it is off (lights are off and the display is blank) but internally the baseband is powered and communication via RBUS is possible. The RF is not powered in acting dead state.

If charger is connected in the off state, the phone enters the acting dead state, but the charging indicator in the UI module shows to the user that the phone is being charged.

Watchdog system

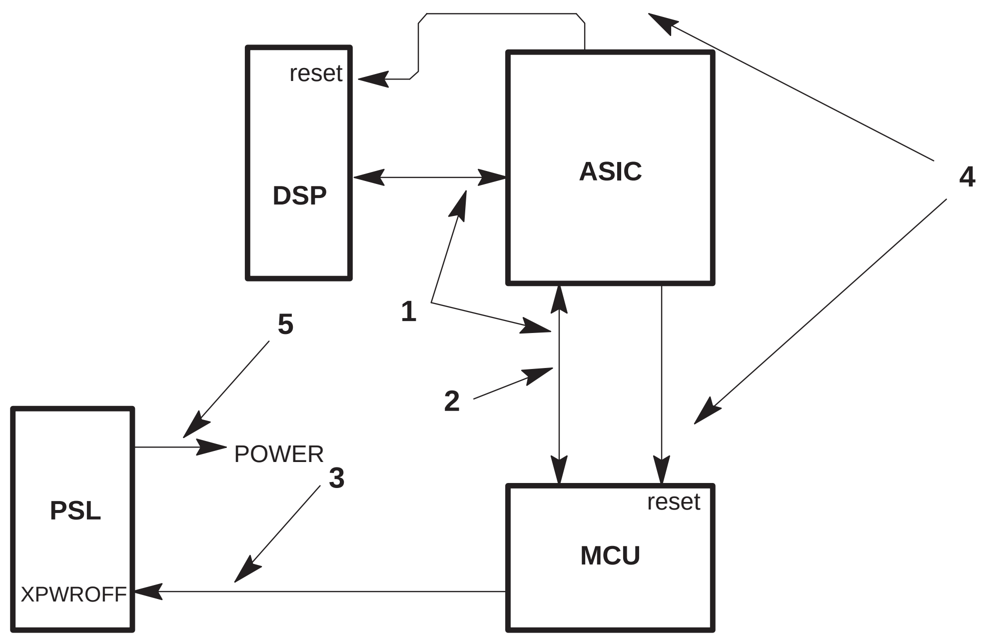

Figure 5. Watchdog system

Normal operation:

1. MCU tests DSP
2. MCU updates ASIC watchdog timer (> 2Hz)
3. MCU pulses the XPWROFF input on the PSL+ (about 2Hz)

Failed operation:

4. ASIC resets MCU and DSP after about 0.5 s failure
5. PSL+ switches power off about 5 s after the previous XPWROFF pulse

CTRLU

Introduction

The Control block contains a microcomputer unit (MCU) and five memory circuits (2xFLASH, 2xSRAM and EEPROM), a 20–bit address bus and a 16–bit data bus. Physically the CTRLU resides entirely on MCM1.

Main Features of the CTRLU Block

MCU functions:

– system control
– communication control
– user interface functions
– GSM data encoding and decoding
– authentication
– RF monitoring
– power up/down control
– accessory monitoring
– battery monitoring and charging control
– self–test and production testing
– flash loading

Technical specifications

Table 23. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Power supply voltage for CTRLU block	PWRU
VREF	Reference voltage for MCU AD–converter	PWRU
VFF	Programming voltage for flash memory	B2B Conn
VBATDET	Battery voltage detection	PWRU
VC	Charger voltage monitoring	PWRU
RESETX	Reset signal for MCU	ASIC
NMI	Non–maskable interrupt request	ASIC
MCUCLK	Main clock for MCU	ASIC
IRQX	Interrupt request	ASIC
PCMCDO	Audio codec control data receiving	AUDIO
TRF	RF–module temperature detection	RF
LID	Cover open/closed detection (HOOK A/D input).	B2B Conn
RBUSRXD	RBUS receive data	B2B Conn
TBAT	Battery temperature monitoring	Battery Conn

Table 23. External Signals and Connections, Inputs (continued)

Signal Name	Signal description	From
BTYPE	Battery size identification	Battery Conn
JCONN	Junction box connection identification	AUDIO
MBUSIN	MBUS RX data	B2B Conn

Table 24. External Signals and Connections, Outputs

Signal Name	Signal description	To
XPWROFF	Power off control, PSL+ watchdog reset	PWRU
PWM	Charger switch on/off control	PWRU
WSTROBEX	MCU write strobe	ASIC
RSTROBEX	MCU read strobe	ASIC
MCUAD(19:16) MCUAD(4:0)	Parts of MCU address bus	ASIC
MRBUSDET	MBUS and RBUS activity detection	ASIC
PCMCLK	Clock for audio codec control data transfer	AUDIO
PCMCDI	Audio codec control data transmitting	AUDIO
XSELPCMC	Chip select for audio codec	AUDIO
RBUSTXD	RBUS transmit	B2B Conn
BACKLIGHT	LCD and display backlight on/off control	B2B Conn
AMP_PWR	PHF amplifier ON/STDBY	AUDIO
VOLTLIM	Charging voltage limitation during call	PWRU
MBUSOUT	MBUS TX data (open drain)	B2B Conn

Table 25. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
MCUDA(15:8)	MCU’s 8–bit data bus	ASIC

Block description

– MCU Memories

The MCU has a 20 bits wide address bus A(19:0) and an 16–bit data bus with memories. The address bits A(19:13) are used for chip select decoding. The decoding is done inside the SCL in CTRLU submodule. Hitachi HD6475388 processor has internal ROM and RAM memories.

Memory Map

Table 26. Memory Map

PAGE	ADDRESS	FPAGE[1:0]= 00	FPAGE[1:0]=01	FPAGE[1:0]=10
0	00000 0EE7F	INTERNAL ROM 60 Kbytes (16 bit)		
	0EE80 0F67F	EXTERNAL ADDRESS SPACE		
	0F680 0FE7F	INTERNAL RAM 2 Kbyte (16 bit)		
	0FE80 0FFFF	REGISTER FIELD 384 bytes		
1	10000 1FFFF	RAM 64 Kbytes (16 bit)		
2 – 11	20000 BFFFF	FLASH 640 Kbytes (16 bit) FA[19:17]=001...101		
12 – 13	C0000 DFFFF	FLASH 128 Kbytes (16 bit) FLASH page 0 FA[19:17]=110	FLASH 128 Kbytes (16 bit) FLASH page 1 FA[19:17]=111	FLASH 128 Kbytes (16 bit) FLASH page 2 FA[19:17]=000
14	E0000 EDFFF	SRAM 56 Kbytes (16 bit)		
	EE000 EFFFF	EEPROM 8 Kbytes (8 bit)		
15	F0000 F001A FFFFF	ASIC 26 bytes (8 bit)		

Table 27. Chip Select Generation

A19	A18	A17	A16	A15	A14	A13	CHIP SELECT	NOTES
0	0	0	1	X	X	X	SRAM (page 1)	32K x 16 bit area
1	1	1	0	0	X	X	SRAM (page 14)	28K x 16 bit area
1	1	1	0	X	0	X	SRAM (page 14)	
1	1	1	0	X	X	0	SRAM (page 14)	
1	1	1	0	1	1	1	EEPROM (page 14)	8K x 8 bit area
1	1	1	1	X	X	X	ASIC (page 15)	64K x 8 bit area
0	0	1	X	X	X	X	FLASH (pages 2 – 3)	320K x 16 bit area
0	1	X	X	X	X	X	FLASH (pages 4 – 7)	
1	0	X	X	X	X	X	FLASH (pages 8 – 11)	
1	1	0	X	X	X	X	FLASH (pages 12 – 13)	64K x 16 bit area, paged with FPAGE[1:0]

Table 28. FLASH address generation on pages 12 – 13

Address and page select inputs					FLASH address (highest bits)			NOTES
A19	A18	A17	FPAGE1	FPAGE0	FA19	FA18	FA18	
1	1	0	0	0	1	1	0	FLASH page 0
1	1	0	0	1	1	1	1	FLASH page 1
1	1	0	1	0	0	0	0	FLASH page 2
1	1	0	1	1	0	0	1	Reset SCL clk divider. **NEVER USE THIS !**

– Flash programming

In flash programming a special flash programming box and a PC is needed. Loading is done through a test connector of PDA module using the same serial channel as RBUS. PDA module should not use RBUS during flash loading. First MCU goes to minimum mode (MBUS command from PC or if MBUS is connected to EXTMIC/JCONN line in power up). Then the flash software is loaded from PC to flash loading box. After the loading is complete the flash loading from box to CMT can be started by MBUS command from PC to the MCU. After that the MCU asks the test box to start flash loading to baseband. The box supplies 12 V programming voltage for flash and starts to send 250 bytes data blocks to the MCU via RBUSRxD line. The baud rate is 406 kbit/s. The MCU calculates the check sum, sends acknowledge via RBUSTxD line and sends the data to flash. When all the data is loaded the CMT makes reset and tells the flash loading box if the loading was succeeded or not. Only PSL+, ASIC, SCL and MCU must be active during the loading.

– CTRLU – PWRU

MCU controls the watchdog timer in PSL+. It sends a positive pulse at approximately 2 Hz to XPWROFF pin of the PSL+ to keep the power on. If MCU fails to deliver this pulse, the PSL+ will remove power from the system. MCU also controls the charger on/off switching in the PWRU block. When power off is requested or MCU leaves PSL+ watchdog without reset. after the watchdog time has elapsed the PSL+ cuts off the supply voltages from the phone.

– CTRLU – ASIC

MCU and ASIC have a common 8–bit data bus and a 9–bit address bus. Bits A(4:0) are used for normal addressing. ASIC controls the main clock, main reset and interrupts to MCU. The 26 MHz MCUCLK is divided by two in SCL and the resulting 13 MHz clock is supplied to the MCU. RESETX resets everything in MCU except the contents of the RAM. IRQX is a general purpose interrupt request line from ASIC. After IRQX request the interrupt register of the ASIC is read to find out the reason for interrupt. NMI is used only to wake up MCU from software standby mode.

– CTRLU – DSPU

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. When power is switched on the MCU loads data from the flash memory to DSP‘s external memory through this mailbox.

– CTRLU – AUDIO

When the the chip select signal XSELPCMC goes low, MCU writes or reads control data to or from the speech codec registers at the rate defined by PCMCLK. PCMCDI is an output data line from MCU to codec and PCMCDO is an input data line from codec to MCU. The AMP_PWR signal is used for switching the Personal Hands–Free amplifier between On and Standby modes.

– CTRLU – RF/BATTERY Monitoring

MCU has internal 12 channel 10 bit AD converter. Following signals are used for monitoring battery, charging and RF:

BTYPE	battery size
TBAT	battery temperature
VBATDET	battery voltage
VC	charging voltage
TRF	RF temperature

– CTRLU – Keyboard and LCD Driver Interface

MCU and User Interface communication is controlled through ASIC.

– CTRLU – ACCESSORIES

MBUS is used to control external accessories. This interface can also be used for factory testing and maintenance purposes.

There are also some control and indication signals for the accessories:

JCONN is used to indicate that junction box is connected. JCONN is actually the DC–level of the EXTMIC signal. Phone can also enter minimum mode when MBUS is connected to EXTMIC line.

Main components

– Hitachi H8/538

H8/538 is a CMOS microcontroller unit (MCU) which includes a static CPU core and on–chip supporting modules with 16–bit architecture. The data bus to outside world is 16 bits wide.

– SCL ASIC
  – MCU address decoding and memory chip select generation
  – FLASH and system ASIC address mapping
  – MBUS interface
  – MBUS/RBUS activity detection
  – MCU clock division from 26 MHz to 13 MHz
– 512k*16bit FLASH memory
  – two 512Kx8 FLASH chips
  – 65 ns maximum read access time
  – contains the main program code for the MCU; part of the DSP program code also located on FLASH
– 64k*16bit SRAM memory
  – two 64Kx8 SRAM chips
  – 65 ns maximum read access time
– 8k*8bit EEPROM memory
  – 150 ns maximum read access time
  – contains user defined information

PWRU

Introduction

The power block creates the supply voltages for the baseband block and contains the charging switch and its control electronics.

Technical description

Table 29. External Signals and Connections, Inputs

Signal Name	Signal description	From
XPWRON	Power on switch	B2B Conn
XPWROFF	PSL+ watchdog updating; power off control	CTRLU
VBATT	Battery voltage	Battery conn

Table 29. External Signals and Connections, Inputs (continued)

Signal Name	Signal description	From
PWM	Charger on/off control	CTRLU
VCHAR	Charging voltage	B2B conn
VOLTLIM	Charging voltage limitation during call; affects HW voltage limit	CTRLU

Table 30. External Signals and Connections, Outputs

Signal Name	Signal description	To
XRES	Master reset	ASIC
VL1	Logic supply voltage. Max 150 mA.	CTRLU, ASIC, RFI, UIF
VL2	Logic supply voltage. Max 150 mA.	DSPU
VA1	Analog supply voltage for AUDIO block. Max 40 mA.	AUDIO
VA2	Analog supply voltage for RFI. Max 80 mA.	RFI
VA3	Analog supply voltage for PHF power amplifier. Max 200 mA.	AUDIO
VREF	Reference voltage 4.65V ∓2%. Max. 5mA.	CTRLU,RF
VBATDET	Switched VBATT divided by 2	CTRLU
CHRDET	Charger detect output	ASIC
VCHARO	Charging voltage to battery	Batt conn
VC	Attenuated VCHAR	CTRLU

Block description

The PSL+ IC produces the following supply voltages:

VL1	150 mA for logic
VL2	150 mA for logic
VA1	40 mA for audios
VA2	80 mA for RFI
VA3	200 mA for PHF booster
VREF	5mA reference

In addition, it has internal watchdog, voltage detection and charger detection functions. The watchdog will cut off output voltages if it is not reset once in every 5 (+/–1?) seconds. The voltage detector resets the phone if the battery voltage falls below 4.8 V (+/–0.2V). The charger detection starts the phone if it is in power–off state when the charging voltage is applied.

The charging electronics is controlled by the MCU. When the charging voltage is applied to the phone and the phone is powered up, the MCU detects it and starts controlling charging. If MCU detects too high charging voltage (over 10 volts) or current (over 78 A/D bit difference between VC and VBATDET) it will cut off the charging. The phone will accept charging voltages from 5 to 13 volts.

If the phone is in power–off state, the PSL+ will detect the charging voltage and turn on the phone. If the battery voltage is high enough the reset will be released and the MCU will start controlling charging. If the battery voltage is too low the phone stays in reset state and the charging control circuitry will pass small charging current to the battery. When the battery voltage has reached 5.5 V (+/– 0.2 V) the reset will be removed and the MCU starts controlling charging.

MCU controls the charging with pulse width modulation output. Charging voltage is limited by hardware in normal operation to 8.9 V and during a call to 7.6 V.

Battery and charging voltages are calibrated in production; 6V is fed to the battery and charger pin and the MCU‘s A/D converter values are stored to EEPROM.

Main components

– PSL+ ASIC (N230)

  Generates voltages, contains power on switch, charger and battery voltage detector and watchdog.

– transistors BCP69–25 (V250), BCV27 (V253,V254), BCW30 (V255) and Schottky STPS340U (V251)

  These components are used for implementing the charging switch.

– transistors BCX51 (V231) and BCP69–25 (V230, V232)

  External output transistors for VL1/VL2 and VA3 regulators in PSL+.

DSPU

Introduction

The DSPU performs of the low–level digital signal processing and control tasks required in channel monitoring and speech and data calls. The DSPU resides physically both in MCM2 (DSP and RAMs) and on CMT motherboard (clock generator and Schottky diode AND gate). Main interfaces of the DSPU:

– MCU via ASIC mailbox

– ASIC

– audio codec

– data bus interface (DBUS) for tracing purposes

– digital audio interface (DAI) for type approval measurements

Main features of the DSP block:

- speech processing
  - speech coding/decoding
    - RPE–LTP–LPC (regular pulse excitation long term prediction linear predictive coding)
  - voice activity detection (VAD) for discontinuous transmission (DTX)
  - comfort noise generation during silence
  - acoustic echo cancellation
- channel coding and transmission
  - block coding (with ASIC)
  - convolutional coding
  - interleaving
  - ciphering (with ASIC)
  - burst building and writing it to ASIC
- Reception
  - reading A/D conversion results from ASIC
  - impulse response calculation
  - matched filtering
  - bit detection (with Viterbi on ASIC)
  - deinterleaving of soft decisions
  - convolutional decoding (with Viterbi)
  - block decoding (with ASIC)
- Adjacent cell monitoring
  - signal strength measurements
  - neighbour timing measurements
  - neighbour parameter reception
- control functions
  - RF controls
    - synthesizer control
    - power ramp programming
    - automatic gain control (AGC)
    - automatic frequency control (AFC)

  – frame structure control
    – control of operations during a TDMA frame (with ASIC)
    – control of multiframe structure
    – channel configuration control
– data functions
  – RLP CRC calculation
  – fax V110 frame encode/decode
– test functions
  – functions for RF measurements
  – debugging functions for product development

Technical description

Table 31. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL2	Logic supply voltage. Max 150 mA.	PWRU
DSPCLKEN	Clock enable for DSP clock oscillator circuit	ASIC
DSP1RSTX	Reset for the DSP	ASIC
PCMDATRCLKX	PCM data input clock DBUS data input clock	ASIC
PCMCOSYCLKX	PCM data bit sync clock	ASIC
CODEC_CLK	PCM data output clock	ASIC
PCMOUT	Received audio in PCM format	AUDIO
DBUSCLK	DBUS data output clock	ASIC
DBUSSYNC	DBUS data bit sync clock	ASIC
RDA	DBUS received data	B2B Conn.
INT0, INT1	Interrupts for the DSP	ASIC

Table 32. External Signals and Connections, Outputs

Signal Name	Signal description	To
PCMIN	Transmitted audio in PCM format	AUDIO
IOX	I/O enable. Indicates access to DSP I/O address space.	ASIC
RWX	Read/Write control	ASIC
DSPAD(16:0)	Address bus and control signals	ASIC
TDA	DBUS transmit data	B2B Conn.

Table 33. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
DSPDA(15:0)	16–bit data bus	ASIC

Block description

The DSPU communicates with the CTRLU through a mailbox in the D2CA ASIC. The software for the external memories are loaded through this mailbox in start up.

The DSP includes two serial buses. One is used for digitized speech transfer between the DSP and the codec. The other is used as an external data bus and it is connected to the B2B connector. This bus can be used for DSP tracing in product development and also as a digital audio interface (DAI) in audio type approval measurements. The clocks (512 kHz main clock and 8 kHz sync. clock) are generated by the D2CA ASIC.

In transmit mode the DSP codes the speech and routes the resulting transmit slots to the D2CA. The D2CA ASIC controls timing, and at specified intervals sends these bits to the RFI for D/A conversion.

In digital receive mode the RFI A/D converts the IF signal from the RF unit under the control of the D2CA. The DSP controls the D2CA and receives the converted samples. The received bits are detected from these samples in DSPU with the aid of some HW accelerators in ASIC. After channel and speech decoding, the bits are converted into an analog signal in the PCM codec. The echo cancellation algorithms of the handportable and Hands–Free modes are also performed in DSPU when needed.

In the case of the data or fax call the DSP performs CRC calculation or FAX V110 frame encoding/decoding instead of the speech encoding/decoding. Channel encoding/decoding and demodulation are performed in DSPU in this case also.

The DSP controls the RF through the D2CA ASIC, where all necessary timing functions are implemented, and control I/O lines are provided eg. for synthesizer loading.

The DSP emulator can be connected to DSP pins TCK, TMS, TDO, TDI, GND and VDD (JTAG standard).

Main components

- AT&T DSP1616–X11
  - Digital signal processor with 12kword internal ROM. The DSP locates physically in MCM2.
- Two 32k *8 70ns SRAMs for DSP external memory. The SRAM's locate physically in MCM2.
- 60.2 MHz crystal oscillator to generate differential small signal clock for the DSP

AUDIO

Introduction

The AUDIO block contains an audio codec and a booster amplifier together with some peripheral components. The codec contains microphone and earpiece amplifiers and all the necessary switches for routing. The codec is controlled by the MCU. The PCM data comes from and goes to the DSP. The booster amplifier for the Personal Hands–Free (PHF) is connected to one of the codec's outputs. Physically the codec resides in MCM2 while the other parts are assembled on the CMT motherboard.

Technical specification

Table 34. External Signals and Connections, Inputs

Signal Name	Signal description	From
VA1	Analog supply voltage. Max 40 mA.	PWRU
VA3	Analog supply voltage for the PHF power amplifier. Max 200 mA.	PWRU
PCMIN	Received audio in PCM format	DSPU
SYNC	8kHz codec frame sync	ASIC
CODEC_CLK	512kHz codec main clock	ASIC
PCMCDI	Audio codec control data	CTRLU
PCMCLK	Clock for audio codec control data transfer	CTRLU
XSELPCMC	Audio codec chip select	CTRLU
AMP_PWR	PHF power amplifier control	CTRLU
MICN, MICP	Differential handportable microphone signal	SIM Conn
EXTMIC	External microphone signal	B2B Conn
PHFMICN, PHFMICP	Differential Personal Hands–Free microphone signal	B2B Conn

Table 35. External Signals and Connections, Outputs

Signal Name	Signal description	To
PCMOUT	Transmitted audio in PCM–format	DSPU
PCMCDO	Audio codec control data	CTRLU
JCONN	Junction box connected signal (multiplexed with EXTMIC)	CTRLU
EARN, EARP	Received audio to the earphone, differential signal	SIMFLEX Conn
EXTEAR	Received audio to the external accessories	B2B Conn
PHFEARN, PHFEARP	Received audio to the Personal Hands–Free speaker, differential signal	PHF Conn

Block description

The codec has three microphone inputs and two earphone outputs. The microphone inputs from handportable and PHF microphones plus the external audio input can be therefore connected directly to the codec. The handportable earphone output and external audio are also connected directly to the codec using the two earphone output channels. The booster amplifier for PFH uses the same codec output channel as the external audio. The codec has internal switches for selecting which input or output is used. It also has microphone amplifier with programmable gain and earphone attenuator with programmable attenuation. Input/output selection and amplification/attenuation setting can be done using codec registers. The registers are controlled by the MCU.

Handportable microphone (MICN, MICP) and PHF microphone (PHFMICN, PHFMICP) are connected directly to the codec‘s differential inputs. There is a bias switch in the AUDIO block, which connects the DC bias voltage for both microphones (electret type) when a call is activated. The external microphone signal (EXTMIC) is connected single–ended to the third microphone input channel. There is 21 dB attenuation in the external microphone line before the codec to prevent clipping.

The handportable’s earphone (EARN, EARP) is connected directly to one of the two differential output channels. The output can drive directly a 32 Ω load. The external audio signal (EXTEAR) is connected single–ended to the other output channel. This output is also connected to the input of the Personal Hands–Free booster amplifier. The booster is disabled by MCU when an external audio accessory is used. In PHF mode, the booster is enabled and its differential output is fed to the PHF speaker (PHFEARN, PHFEARP). The load impedance of the PHF speaker is 8 Ω.

Inside the codec, the currently selected microphone signal is routed to the microphone amplifier. After that it is fed to the bandpass filter and then to the A/D converter. After the conversion the digital speech is sent to the DSP in PCM format.

Digital downlink signal from the DSP is fed to the D/A converted. After the converter there is low pass filter and attenuator before the earphone output. All these are inside the codec. The ASIC generates the 512 kHz and 8 kHz clocks for the codec and data transmission between the codec and the DSP.

The audio codec communicates with the DSP (digital speech) through an SIO (signals: PCMIN, SYNC, CODEC_CLK and PCMOUT).The MCU controls the audio codec function through a separate serial bus (signals: PCMCDO, PCMCDI, PCMCLK and XSELPCMC). The PHF power amplifier can be enabled or disabled using the AMP_PWR signal from the MCU. The power amplifier is enabled only when needed due to power consumption reasons.

The codec generates DTMF tones (key beeps) to the earphone and in PHF mode to the PHF speaker. When an external audio accessory is used, the DTMF tones are directed to the external audio output. In handportable and PHF modes the codec generates ringing tones and also some warning tones to the PHF speaker. In external HF mode they are driven to the external speaker line. Some tones come also from the network.

One codec output pin is used to switch on/off the microphone bias circuit. Both microphones are biased simultaneously regardless of which one is actually used.

External microphone line is used also to detect if the junction box is connected to the bottom connector. Microphone signal is therefore low–pass filtered and routed to the MCU A/D converter named as the JCONN signal.

Also external earphone signal is multiplexed. 100 kohm pull down resistor is used to turn power on to the HF accessories.

Main components

– Audio codec ST5090

  Contains e.g. PCM codec, audio routing switches, 3 differential microphone input channels, 2 differential earpiece output channels, ringing tone and DTMF generators. Physically the codec is inside MCM2.

– Power amplifier LM4861 (N400)

  Used as the booster amplifier for Personal Hands–Free.

– Transistors BC859C (V380) and BC849C (V381)

  Used for implementing the microphone bias switch.

ASIC

Introduction

The ASIC takes care of the following functions:

– interface between MCU and UIF
– interface between MCU, DSP and RFI
– hardware accelerator functions to DSP
– clock generation and disable/enable
– RF controls
– UIF interface
– Timers
– MBUS or RBUS activity detection
– SIM interface

Physically the D2CA ASIC is located in MCM2. The VCXO clock buffer and SIM power switch are assembled on CMT motherboard.

Technical specification

Table 36. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Logic supply voltage. Max 150 mA.	PWRU
IOX	I/O enable. Indicates access to DSP I/O address space.	DSPU
RWX	Read/WriteX	DSPU
WSTROBEX	MCU's write strobe	CTRLU
RSTROBEX	MCU's read strobe	CTRLU
RFC	Reference clock from VCXO (26 MHz)	RF
XRES	Master reset	PWRU
DSPAD(16:0)	DSP's address bus and control signals	DSPU
MCUAD(19:16,4:0)	MCU's address bus	CTRLU
DAX	Data acknowledge	RFI
MRBUSDET	MBUS/RBUS activity detection	CTRLU
DBUSDET	DBUS activity detection	DSPU

Table 37. External Signals and Connections, Outputs

Signal Name	Signal description	To
INT0, INT1	Interrupts for DSP	DSPU
NMI	Not maskable interrupt request	CTRLU
IRQX	Interrupt request	CTRLU
RESETX	Master (power up) reset	CTRLU, RFI
DSP1RSTX	Reset for the DSP	DSPU
SIMRESET	Reset for the SIM	SIMFLEX conn
WRX	Write strobe	RFI
RDX	Read strobe	RFI
RFIAD(3:0)	RFI address bus	RFI
SCLK	Synthesizer load clock	RF
SDATA	Synthesizer load data	RF
SENA1	UHF and VHF PLL enable	RF
RXPWR	RX circuitry power enable	RF
TXPWR	TX circuitry power enable	RF
SYNTHPWR	Synthesizer circuitry power enable	RF
TXP	Transmitter power control enable	RF
MCUCLK	Main clock for MCU (26 MHz)	CTRLU

Table 37. External Signals and Connections, Outputs (continued)

Signal Name	Signal description	To
DSPCLKEN	DSP clock circuit enable	DSPU
RFICLK	RFI master clock (13 MHz)	RFI
RFI2CLK	RFI sleep clock (135.4 kHz)	RFI
CODEC_CLK	PCM data clock (512 kHz)	DSPU, AU-DIO
PCMDATRCLKX	Inverted PCM data clock (512 kHz) used as input clock for Codec and DBUS interface	DSPU
SYNC	Bit sync clock (8 kHz)	AUDIO
PCMCOSYCLKX	Bit sync clock (8 kHz), inverted	DSPU
DCLK	DBUS data clock (512 kHz)	DSPU
DSYNC	DBUS bit sync clock (8 kHz)	DSPU
SIMCLK	SIM data clock (3.25/1.625 MHz)	SIMFLEX Conn.
VSIM	SIM power control	SIMFLEX Conn.
COL(3:0)	Lines for keyboard column write	B2B Conn.

Table 38. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
DSPDA(15:0)	DSP’s 16–bit data bus	DSPU
MCUDA(15:8)	MCU’s 8–bit data bus	CTRLU
RFIDA(11:0)	RFI’s 12–bit data bus	RFI
UIF(6:0)	LCD–controller control and keyboard read bus	B2B Conn.
SIMDATA	Serial data from/to SIM	SIMFLEX Conn.

Block description

PSL+ supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. MCU and RFI reset is released after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13MHz clock cycles. In our case 255 is selected. SIM reset release time is according to GSM SIM specifications.

The RFC buffer buffers the 26 MHz clock from theVCXO to the ASIC. In the ASIC the clock is further buffered and delivered to MCU. The clock is also divided and delivered to RFI and SIM. ASIC also generates main and sync clocks for audio codec, DSP‘s SIOs and DBUS. The clock outputs can be disabled in order to save current when the clock is not needed. Also the 60.2 MHz DSP oscillator can be disabled by the ASIC.

Interface to the MCU is done with 8 bit data bus, 5 bit lower address bus, 4 bit upper address bus, RSTROBEX, WSTROBEX, IRQX and NMI. ASIC is in the same memory space as MCU memories. There is also MBUS/RBUS detector and netfree counter on the ASIC. Netfree interrupt IRQX occurs if no activity is detected in MBUS in about 3 ms. ***Note**: This netfree counter cannot be used in the CMT because RBUS data is seen at the same pin*. NMI is used to wake up the MCU from sleep mode.

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. The size of the mailbox is 64 * 8 bit.

MCU and User Interface (keyboard and display) communication is controlled through the ASIC. COL(3:0) are used as column lines in keyboard. UIF(5:0) are used as row lines They are also multiplexed with display driver control signals.
When a key is pressed the ASIC gets a reset from row and starts scanning. One column at the time is written to low and rows are used to read which key it was. Row lines and UIF6 are used for display driver control. UIF(3:0) are used as 4 bit parallel data bus for the LCD driver. UIF4 is used as read/write strobe, UIF5 to select data or instruction register and UIF6 as enable strobe.

The SIM interface is the electrical interface between the SIM (the smart card used in the GSM and PCN applications) and the MCU via the ASIC. ASIC converts the serial data received from the SIM to parallel data for MCU and converts parallel data from MCU to serial mode for the card. The SIM interface also takes care of the power up and down procedure to the card in addition to frame and parity error checking. The communication between card and ASIC is asyncronous and half duplex.Four signals are used between the ASIC and the SIM card: SIMDATA, SIMCLK,SIMRESET and VSIM. The nominal clock frequency is 3.25 MHz. When there is no data transfer between the SIM card and the CMT the clock can be reduced to 1.625 MHz. Some SIM cards also allow the clock to be stopped in that mode. Supply voltage VSIM can be switched off by the ASIC. The supply voltage range is 4.65–4.95 V. The card detect input of the ASIC is connected to BTYPE pin and when the battery is removed the ASIC will drive the SIM down.

The interface to the DSP is done using 6 bit address bus, 16 bit data bus, IOX and RWX lines. Data bus is latched using IOX, address bus is not. The ASIC also generates interrupt INT0 when an edge occurs in DBUS line (if the mask bit is off). INT1 is used as RX interrupt and as MFI modulator interrupt to the DSP.

Viterbi is used to perform GSM/PCN convolutional decoding and bit detection according to the Viterbi algorithm. It can be controlled and accessed thoroughly by the DSP.

Coder is used to perform block encoding, decoding, and ciphering according to GSM algorithms A5 and A5/2.

The ASIC takes care of the interface between the DSP and the RFI: TX modulator, RX filter, TX and RX sample buffers and controlling state machine. The interface to RFI is done using 12 bit data bus, 4 bit address bus, RDX and WRX. There is also data acknowledge (DAX) signal from RFI to ASIC. Also in this block is the serial RF synthesizer interface (SCLK, SDAT, SENA1) and the digital RF control signals (RXPWR, TXPWR, TXP, SYNTHPWR)

Main components

– D2CA ASIC, physically in MCM2
– 2 x TC7S00F (D300,D301) NAND gate
  Inverter buffer stage is used for converting the low–level VCXO clock to valid logic levels.
– Transistors BC848W (V330) and BCW30 (V331)
  The SIM power switch.

RFI

Introduction

The RFI block consists of the RFI ASIC and its reference voltage generator. This block is an interface between the RF and baseband sections. The RFI block has the following functions:

– IF receiving and A/D conversion
– I/Q separation
– I– and Q–transmit and D/A conversion
– AFC D/A conversion
– TXC D/A conversion (burst template)
– analog AGC and digital LNA gain switch

Technical specification

Table 39. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Logic supply voltage. Max 150 mA.	PWRU
VA2	Analog supply voltage. Max 80 mA.	PWRU
RESETX	Master (power up) reset	PWRU
RFIAD(3:0)	RFI address bus	ASIC
RDX	Read strobe	ASIC
WRX	Write strobe	ASIC
RFICLK	RFI master clock	ASIC
RFI2CLK	RFI sleep clock	ASIC
RXQ	RX quadrature signal	RF
RXI	RX in–phase signal	RF

Table 40. External Signals and Connections, Outputs

Signal Name	Signal description	To
DAX	Data acknowledge	ASIC
AFC	Automatic frequency control voltage	RF
TXC	TX transmit power control voltage / RX AGC voltage	RF
TXQP,TXQN	differential TX quadrature signal	RF
TXIP,TXIN	differential TX in–phase signal	RF
PDATA0	LNA gain reduction	RF

Table 41. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
RFIDA(11:0)	12–bit data bus	ASIC

Block description

The RFI provides A/D conversion of the in–phase (RXI) and quadrature (RXQ) signals in receive path. It has 12 bit A/D converters and the output sample rate is 541.667 kHz.

Analog transmit path includes 8 bit D/A converters to generate the in–phase (TXI) and quadrature (TXQ) signals. RFI has differential outputs for TXI and TXQ. The sample rate is 1.0833 MHz.

There is an 11 bit D/A converter for automatic frequency correction (AFC). The sample rate is 1.3542 kHz.

Power ramp (TXC) is done with 10 bit D/A converter. The sample frequency is 1.0833 MHz. This converter is also used for AGC during receive slots.

The PDATA0 signal is used for LNA gain reduction in strong field conditions. The rest of the AGC control is analog. The analog AGC (used in receive) is multiplexed with the TXC signal (used in transmit).

The RFI has 12 bit data bus to the ASIC. The registers in the RFI are accessed using 4 address bits. Control and clock signals are coming from the ASIC.

The RFI has external 4.096 V voltage reference.

Main components

– RFI ASIC, physically in MCM2

– 4.096 V external voltage reference LM4040 (V420)

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Chapter 3
–Transceiver GE8/GE9 –
RF Block

CONTENTS –RF

List of Figures

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Introduction

The RF module for Responder is taken from the HD841 project with only minor modifications in the built–in and external antenna interfaces. Otherwise the circuitry and layout are almost completely the same as in HD841 GSM and PCN versions.

Technical Summary

The RF module carries out all the RF functions of the transceiver. The GSM and PCN systems use different RF modules. The mechanical size of both modules is the same.

EMI leakage is prevented with magnesium shield B on side one and metallised plastic shield A on side two. Shield B conducts also heat out of the inner parts of the phone thus preventing excessive temperature rise.

External Signals and Connections

Table 1. List of Connectors

Connector Name	Code	Notes	Specifications / Ratings
Built–in antenna connector	5429003	SMD coaxial connector for Whip or Helix antenna	50 Ω / 2.0 W
External antenna connector	5420460	Includes antenna switch	50 Ω / 2.0 W

Main Technical Specifications

RF frequency plan

GSM

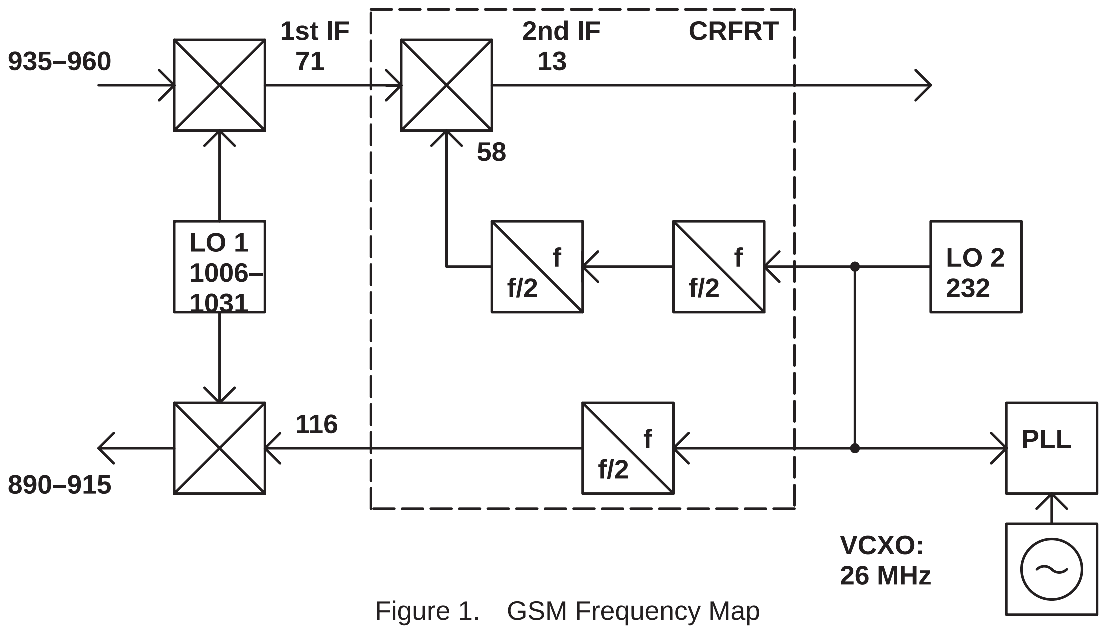

Figure 1. GSM Frequency Map

PCN

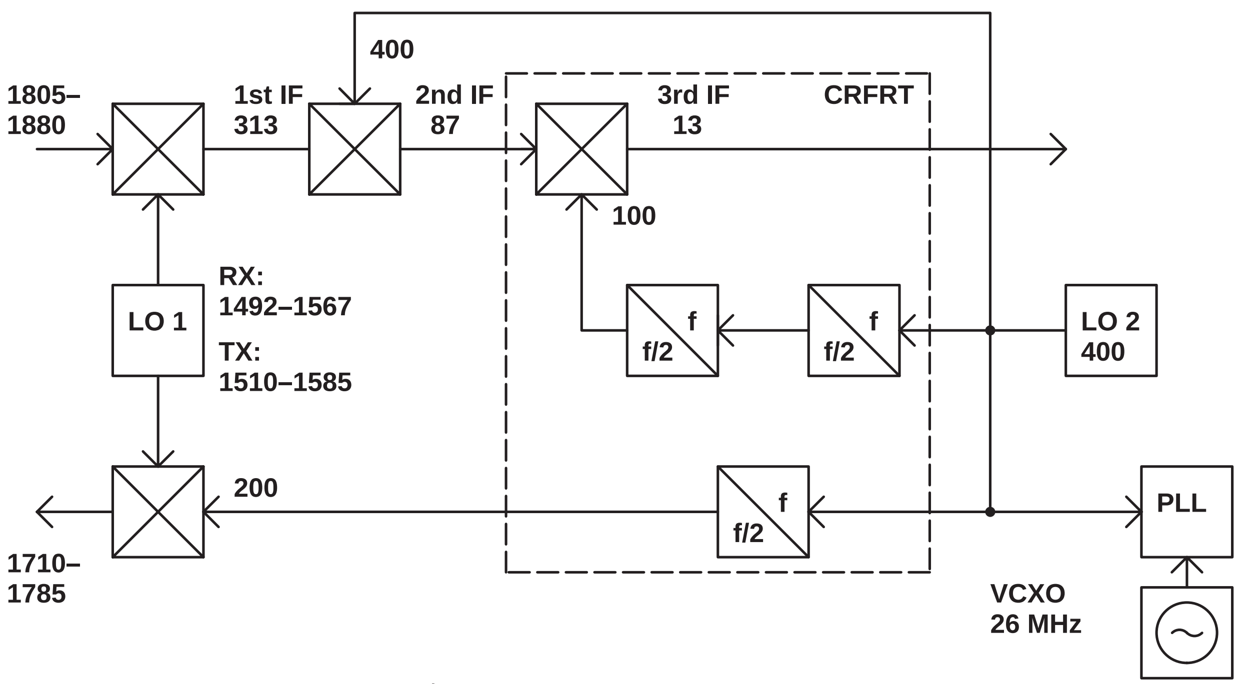

Figure 2. PCN Frequency map

Maximum Ratings

The maximum battery voltage during the transmission should not exceed 8.5 V. Higher battery voltages may destroy the power amplifier. During charging this will be quaranteed by hardware based limiting which has maximum value 7.6 +/–0.3 V. However, the maximum voltage of the Li–Ion battery will be almost 8.5 V when the battery is full. The charging algorithm ensures that the voltage never exceeds this limit.

Power Distribution Diagram

GSM/PCN:

All currents in the power distribution diagram are peak currents. Activity percentages are in CALL–mode 24.6 % for RXPWR, 15.8 % for TXPWR and 100 % for SYNTHPWR. In IDLE–mode activities are 0.4 %, 0.0 % and 1.77 % respectively. The current of each block is controlled independently, for example TXPWR and RXPWR are not on at the same time.

Regulators

There is one regulator IC in the RF unit. The regulator IC CRFCONT is an RF power supply circuit basically intended for digital handportable phones. It has 8 separate linear regulators and power on/off switches for RF–circuitry. Each regulator can be individually disabled and enabled and also has a voltage reference output.

See more details on Figure 3 and Figure 4.

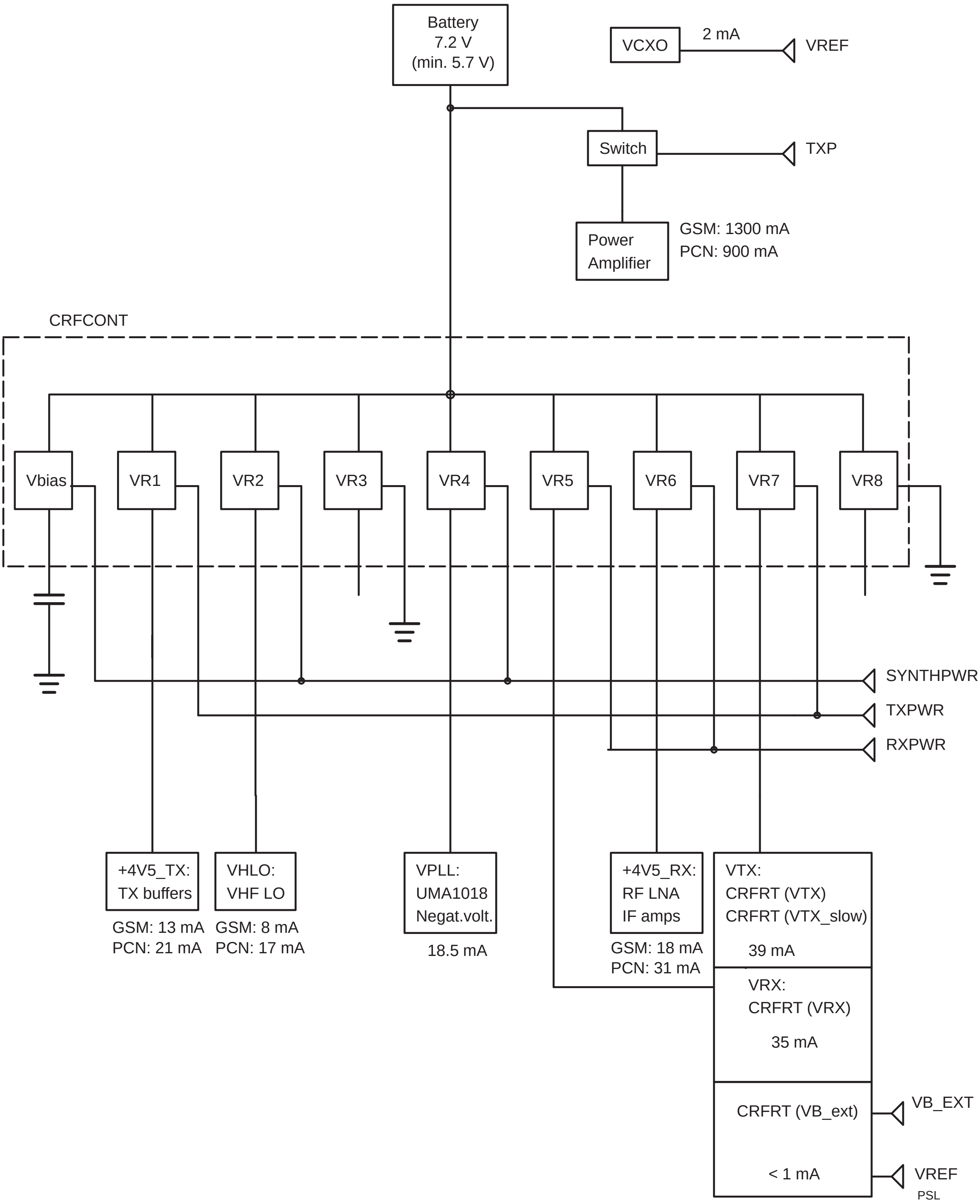

Figure 3. Power distribution diagram

Control Signals

In the following tables (Table 2, 3, 4) the RF current consumption can be seen with different status of the control signals. The VCXO current is not included in the results.

Table 2. Control Signals and Current Consumption

GSM,PCN					
SYNTHPWR	**RXPWR**	**TXPWR**	**TXP**	**Typical load current / mA**	**Notes**
L	L	L	L	0.05	Leakage current
H	L	L	L	42	Synthesizers active
H	H	L	L	116	Reception
H	L	H	L	94	TX active
H	L	H	H	1400	Transmission (GSM)
H	L	H	H	800	Transmission (PCN)

Functional Description

Receiver

The GSM receiver is a double conversion receiver. The PCN receiver has three conversions.

The received RF signal from the antenna is fed via a duplex filter to the receiver unit. The signal is amplified by a discrete low noise preamplifier. The gain of the amplifier is controlled by the AGC control line (PDATA0). The nominal gain of 10 dB in PCN is reduced in the strong field condition about 24 dB and in GSM the nominal gain of 16.5 dB is reduced about 36 dB. After the preamplifier the signal is filtered by ceramic (PCN) or SAW (GSM) RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the receiver unit.

In PCN the filtered RF–signal is down converted by a passive diode mixer. The frequency of the first IF is 313 MHz. The first local signal is generated by the UHF synthesizer. The IF signal is amplified and then filtered by a microstripline filter. The filtered 1st IF is down converted by the second mixer, which is also a passive diode mixer. The 2nd IF frequency is 87 MHz. The 2nd local signal is generated by the VHF synthesizer.

In the GSM system the filtered RF–signal is also down converted by the passive diode mixer. The first IF frequency is 71 MHz and the first local signal is generated by the UHF synthesizer.

All the IF signals 71 and 87 MHz are amplified and filtered by SAW filter in GSM and PCN . The filter rejects adjacent channel signal, intermodulating signals and the last IF image signal.

The filtered IF signal is fed to the receiver part of the integrated RF circuit CRFRT. In CRFRT the filtered IF signal is amplified by an AGC amplifier which has gain control range of 57 dB. The gain is controlled by an analog signal via TXC–line. The amplified IF signal is down converted to the last IF in the mixer of CRFRT. The last local signal is generated from VHF VCO by dividing the original signal by 4 in the dividers of CRFRT.

The last IF frequency is 13 MHz in GSM and PCN. The last IF is filtered by a ceramic filter. The filter rejects signals of the adjacent channels. The filtered last IF is fed back to CRFRT where it is amplified. Finally the IF signal is split to +45 and –45 signals and then fed to RFI.

The block diagram overleaf, Figure 4., is common for GSM and PCN. Blocks in parenthesis refer to PCN only. In GSM these parts do not exist and in the signal path are replaced by direct connection to the next block.

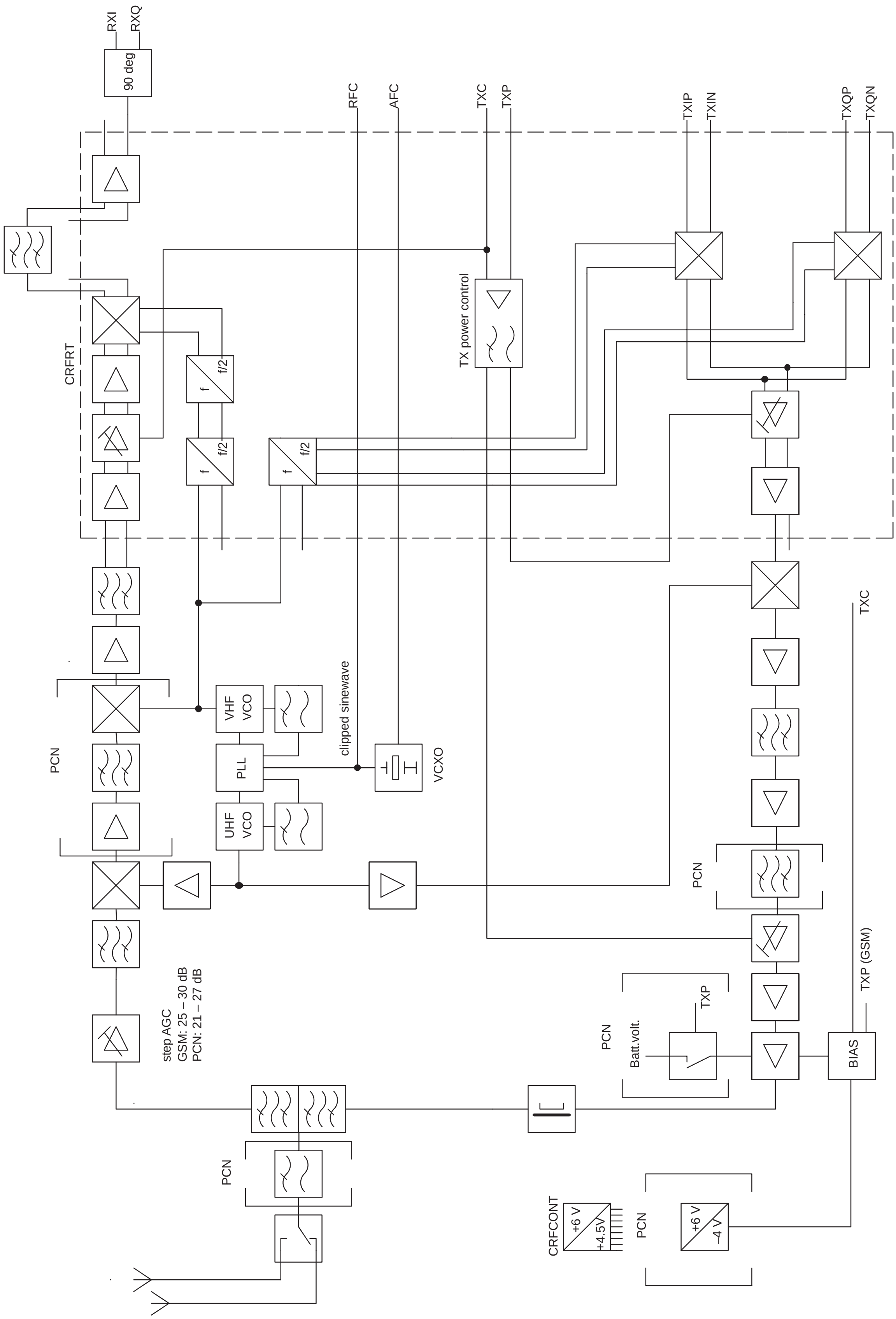

Figure 4. RF Functional Block diagram

Frequency Synthesizers

The stable frequency source for the synthesizers and base band circuits is discrete voltage controlled crystal oscillator (VCXO) in GSM and PCN.The frequency of the oscillators is controlled by an AFC voltage, which is generated by the base band circuits. The VCXO is always running when the CMT is powered up. The nominal frequency is 26 MHz in GSM and PCN.

The UHF PLL generates the down conversion signal for the receiver and the up conversion signal for the transmitter.

The VHF PLL signal (divided by 4 in CRFRT) is used as a local oscillator for the last mixer. Directly it is used as a second local oscillator in PCN. The VHF PLL signal (divided by 2 in CRFRT) is also used in the I/Q modulator of the transmitter chain. The VHF VCO is made of discrete components.

Transmitter

The TX intermediate frequency is modulated by an I/Q modulator contained on transmitter section of CRFRT IC. The TX I and Q signals are generated in the RFI interface circuit and they are fed differentially to the modulator.

Modulated intermediate signal is amplified or attenuated in temperature compensated controlled gain amplifier (TCGA). The output of the TCGA is amplified and the output level is typically –10dBm.

The output signal from CRFRT is band–pass filtered (in PCN low–pass filtered) to reduce harmonics and the final TX signal is achieved by mixing the UHF VCO signal and the modulated TX intermediate signal with passive mixer. After mixing the TX signal is amplified and filtered by two amplifiers and filters except in GSM there is only one filter. These filters are dielectric filters in both GSM and PCN. After these stages the level of the signal is typically 1 mW (0 dBm) in GSM and 2 mW (+3 dBm.) in PCN.

The discrete power amplifier amplifies the TX signal to the desired power level. The maximum output level is typically 1.5...2.0 W in GSM and 0.8...1.0 W in PCN in the antenna terminal of the duplex filter.

The power control loop controls the output level of the power amplifier. The power detector consists of a directional coupler and a diode rectifier. Transmitted power is controlled with TCGA on TX–path of CRFRT. Power is controlled with TXC and TXP signals. The power control signal (TXC), which has a raised cosine form, comes from the RF interface circuit (RFI), which is located in the baseband section.

RF Characteristics

Receiver

Table 3. RF characteristics, Receiver

Item	GSM	PCN
RX frequency range , MHz	935 ... 960	1805 ... 1880
Type	Linear, 2 IFs	Linear, 3 IFs
Intermediate frequencies , MHz	71 , 13	313, 87, 13
3 dB bandwidth ,kHz	+/– 100	+/– 100
Reference noise bandwidth ,kHz	270	270
Sensitivity , dBm	–102, S/N ratio > 8 dB, B_N = 135 kHz	–100 , S/N ratio > 8 dB, B_N =135 kHz
AGC dynamic range dB	85 , typ	81 , typ.
Receiver gain ,dB	69 , typ	67 , typ
RF front end gain control range,dB	36	24
2nd IF gain control range, dB	57	57
Input dynamic range ,dBm	–100 ... –10	–100 ... –10
Gain relative accuracy in receiving band, dB	+/–1.5	+/– 1.5
Gain relative accuracy on channel, dB	+/–0.4	+/– 0.4

Duplex filter

The duplex filter consists of two functional parts; RX and TX filters. The TX filter rejects the noise power at the RX frequency band and TX harmonic signals. The RX filter rejects blocking and spurious signals coming from the antenna. In PCN there is a lowpass filter between the duplexer and RF connector, which further improves the spurious response rejection above 2 GHz.

Pre–amplifier

The bipolar pre–amplifier amplifies the received signal coming from the antenna. In the strong field conditions the gain of the amplifier is reduced 36 dB in GSM and 24 dB in PCN, typically.

Table 4. Pre amplifier specifications

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
Frequency band	GSM PCN		935–960 1805 – 1880		MHz MHz
Supply voltage		4.27	4.5	4.73	V
Current consumption	GSM PCN	5 4	6 5.5	7 8	mA mA
Insertion gain	GSM PCN	15 8	16.5 10	17 12	dB dB
Gain flatness			+/– 0.5		dB
Noise figure	GSM PCN		2.0 2.3	2.5 2.8	dB dB
Reverse isolation		15			dB
Gain reduction	GSM PCN	33 21	36 24	39 27	dB dB
IIP3	GSM PCN	–12 –12	–10 –10		dBm dBm
Input VSWR (Zo=50 ohms)				2.0	
Output VSWR (Zo=50 ohms)				2.0	

RX Interstage Filter

The RX interstage filter is a three pole ceramic filter in PCN. In GSM there is a SAW filter. The filter rejects spurious and blocking signals coming from the antenna. It also rejects the local oscillator signal leakage.

First mixer

The first mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer down converts the received RF signal to the first IF signal.

Table 5. Mixer Specification

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
RX frequency range	GSM PCN	935 1805		960 1880	MHz MHz
LO frequency range	GSM PCN	1006 1492		1031 1567	MHz MHz
IF frequency	GSM PCN		71 313		MHz MHz
Conversion loss		5	6	7	dB

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
IIP3	GSM PCN	2 2	5 5		dBm dBm
LO – RF isolation		15.0			dB
LO power level		3			dBm

First IF amplifier

The first IF amplifier is a bipolar transistor amplifier.

Table 6. 1st IF amplifier specification

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
Operation frequency	GSM PCN		71 313		MHz MHz
Supply voltage		4.27	4.5	4.73	V
Current consumption	GSM PCN		12 5.5	15 10	mA mA
Insertion gain	GSM PCN	18 12	20 14	22 18	dB dB
Noise figure	GSM PCN		3.5 2.5	4.0 3.0	dB dB
IIP3	GSM PCN	–5 –5	–3 –3		dBm dBm
Input impedance					matched to the mixer
Output impedance	GSM PCN				matched to the filter matched to the mixer

First IF filter

The first IF filter is a microstripline filter in PCN. In GSM the first IF filter is a SAW filter. The IF filter rejects some spurious and blocking signal coming from the front end of the receiver.

2nd mixer (only in PCN)

The 2nd mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer down converts the 1st IF signal 313 MHz to 2nd IF signal 87 MHz.

Table 7. 2nd Mixer Specification (PCN)

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
1st IF frequency		313		MHz
LO frequency		400		MHz
2nd IF frequency		87		MHz
Conversion loss	5	6	7	dB
IIP3	2	5		dBm
LO – RF isolation	15.0			dB
LO power level	3			dBm

2nd IF amplifier (only in PCN)

The 2nd IF amplifier is realized using resistive feedback connection for bipolar RF transistor.

Table 8. 2nd IF amplifier specification (PCN)

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operation frequency		87		MHz
Supply voltage		4.5		V
Current consumption		11	15	mA
Insertion gain	14	16	18	dB
Noise figure		2.5	3.0	dB
IIP3	–3	0		dBm
Input impedance				matched to the mixer
Output impedance				matched to IF filter

2nd IF filter (only in PCN)

The second IF filter (SAW) makes the part of the channel selectivity of the receiver. It rejects adjacent channel signals (except the 2nd adjacent). It also rejects blocking signals and the 3rd image frequency.

Receiver IF circuit, RX part of CRFRT

The receiver part of CRFRT consists of an AGC amplifier of 57 dB gain, a mixer and a buffer amplifier for the last IF. The mixer of the circuit down converts the received signal to the last IF frequency. After external filtering the signal is amplified and fed to baseband circuitry. The supply current can be switched OFF by an internal switch, when the RX is OFF.

Table 9. CRFRT RX part Specifications

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.27	4.5	4.73	V
Current consumption		32.0	44.0	mA
Input frequency range	41 (–1 dB)		87 (–3 dB)	MHz
Local frequency range of mixer	170		400	MHz
2nd IF range	2		17	MHz
Voltage gain (max. gain) of AGC amplifier	47			dB
Noise figure			16	Max gain
AGC gain control slope	40	84	100	dB/V
Mixer output 1dB compression point		1.0		Vpp
Max output level after last IF buffer		1.6		Vpp

Last IF filter

The last IF is a ceramic filter, which makes the part of the channel selectivity of the receiver.

Transmitter

Table 10. RF Characteristics, Transmitter

Item	GSM	PCN
TX frequency range	890...915 MHz	1710...1785 MHz
Type	Upconversion	Upconversion
Intermediate frequency	116 MHz	200 MHz
Maximum output power	2 W (33 dBm)	1 W (30 dBm)
Gain control range	20 dB	20 dB
Maximum RMS phase error	5 deg.	5 deg.

Modulator Circuit, TX part of CRFRT

The modulator is a quadrature modulator contained in Tx–section of CRFRT IC. The I– and Q– inputs generated by RFI interface are DC–coupled and fed via buffers to the modulator. The local signal is divided by two to get accurate 90 degrees phase shifted signals to the I/Q mixers. After mixing the signals are combined and amplified with temperature compensated controlled gain amplifier (TCGA). Gain is controlled with power control signal (TXC). The output of the TCGA is amplified and the maximum output level is –10 dBm, typically.

Table 11. CRFRT TX–part specifications

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.27	4.5	4.73	V
Supply current		36	45	mA
Transmit Frequency Input	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
LO input frequency	170		400	MHz
LO input level		0.2		Vpp
LO input resistance	70	100	130	ohm
LO input capacitance		4		pF
Modulator Inputs (I/Q)	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Input bias current (balanced)			100	nA
Input common mode voltage	2.0	2.2	2.4	V
Input level (balanced)			1.1	Vpp
Input frequency range	0		300	kHz
Input resistance (balanced)	200			kohms
Input capacitance (balanced)			4	pF
Output frequency	85		200	MHz

Table 11. CRFRT TX–part specifications (continued)

Modulator Inputs (I/Q)	Minimum	Typical / Nominal	Maximum	Unit / Notes
Available linear RF power		–10		dBm, ZiL=50 ohms
Available saturated RF power	–5	0		dBm, ZiL=50 ohms
Total gain control range	45			dB
Gain control slope		84		dB/V
Suppression of 3rd order prods	35			dB
Carrier suppression		35		dB
Single sideband suppression				dB
Noise floor Pout = –10 dBm			–132	dBm/Hz avg.
Noise floor Pout = –18 dBm			–137	dBm/Hz avg.
Noise floor Pout = –24 dBm			–140	dBm/Hz avg.
Noise floor Pout = –30 dBm			–142	dBm/Hz avg.
Noise floor Pout = –40 dBm			–144	dBm/Hz avg.
TX I/Q phase balance Tolerance over temp. range	–5 –2		5 2	deg deg
TX I/Q amplitude balance Tolerance over temp. range	–0.5 –0.2		0.5 0.2	dB dB

Upconversion mixer

The upconversion mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer upconverts the modulated IF signal coming from quadrature modulator to RF signal.

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
RX frequency range	GSM PCN	890 1710		915 1785	MHz MHz
LO frequency range	GSM PCN	1006 1510		1031 1585	MHz MHz
IF frequency	GSM PCN		116 200		MHz MHz
Conversion loss		6.0	7.0	8.0	dB
IIP3	GSM PCN	0.0 0.0			dBm dBm
LO – RF isolation		15.0			dB
LO power level	GSM PCN			3.0 3.0	dBm dBm

1st TX buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the upconversion mixer.

Table 12. 1st TX amplifier specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operating freq. range GSM PCN	890 1710		915 1785	MHz MHz
Supply voltage	4.25	4.5	4.8	V
Current consumption GSM / PCN		4.5	5.0	mA
Insertion gain GSM PCN	11 10	12 11	13 12	dB dB
Input VSWR (Zo=50 ohms)			2.0	Matched to the mixer
Output VSWR (Zo=50 ohms)			2.0	

TX interstage filters

The TX filters reject the spurious signals generated in the upconversion mixer. They also reject the local, image and IF signal leakage and RX band noise.

2nd TX buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the first interstage filter.

Table 13. 2nd TX amplifier specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operating freq. range GSM PCN	890 1710		915 1785	MHz MHz
Supply voltage	4.25	4.5	4.8	V
Current consumption GSM PCN		9.0 16.0	10.0 17.0	mA mA
Insertion gain GSM PCN	11 15	12 16	13 17	dB dB
Output power (Zo=50 ohms) GSM PCN	 0 2	 3 7		 dBm dBm
Input VSWR (Zo=50 ohms)			2.0	
Output VSWR (Zo=50 ohms)			2.0	

Power amplifier

The power amplifier is a three stage discrete amplifier. It amplifies the 0 dBm (2 dBm in PCN) TX signal to the desired output level. It has been specified for 5.5...8.5 volts operation. There are 5 x 330 μF capacitors in the near vicinity of the power amplifier to alleviate supply voltage degradation during TX burst.

Table 14. Power amplifier specification

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
DC supply voltage (no RF)				10	V
DC supply voltage		5.5	7.2	8.5	V
Operating frequency range					
	GSM	890		915	MHz
	PCN	1710		1785	MHz
Operating case temp. range					
	GSM			90	deg.C
	PCN			90	deg.C
Max Output power	GSM PCN	34.5 31.5	35 33	36 34.5	dBm, normal cond dBm, normal cond
Max Output power	GSM PCN	33.5 31	34 32.5	35 34	dBm, extreme cond. Vcc=5.4V, Ta = 55 C
Input power	GSM PCN	0 2			dBm dBm
Gain	GSM PCN	34.5 29.5	35 31	36 32.5	dB, normal cond dB, normal cond
Efficiency	GSM PCN		42 38		%, Pout = 35 dBm %, Pout = 32 dBm
Input VSWR (Zo=50 ohms)				2.0	
Output VSWR (Zo=50 ohms)				2.0	
Harmonics:	$2 f_0$ $3 f_0$, $4 f_0$, $5 f_0$			–30 –40	dBc, Pout = 35 dBm dBc, Pout = 32 dBm
Noise power	GSM PCN			–114 –114	dBm/Hz at RX band dBm/Hz at RX band
Ruggedness	VBATT GSM VBATT PCN	8.0 V T.B.D.			VSWR=7, Pout=4W T.B.D.
Stability (load VSWR 8:1)				–60	dBc, all spurious

Power control circuitry

The power control loop consists of a power detector and a differential control circuit. The power detector is a combination of a directional coupler and a diode rectifier. The differential control circuit compares the detected voltage and the control voltage (TXC) and controls voltage controlled amplifier (in CRFRT) or the power amplifier. The control circuit is a part of CRFRT.

Table 15. Power control specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage using CRFRT	4.5 4.27	4.7 4.5	4.9 4.73	V V
Supply current using CRFRT		3.0	5.0	mA
Power control range GSM PCN	20 20			dB dB
Power control inaccuracy GSM PCN	 - -		 +/–1.0 +/–1.0	 dB dB
Dynamic range GSM PCN	80 80			dB dB
Input control voltage range GSM PCN	 0.1 0.1		 2.8 2.8	 V

Synthesizers

Reference oscillator

In GSM and PCN the reference oscillator is a discrete VCXO and the frequency is 26 MHz. In PCN the buffer amplifier for the reference oscillator is located in the RF side near the local oscillator, although it is drawn in the baseband schematic.

The oscillator signal is used for a reference frequency of the synthesizers and the clock source for the baseband circuits.

Table 16. VCXO specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Center frequency		26		MHz
Frequency tolerance				ppm, Vc=2.2 V
Frequency control range		67		ppm
Supply voltage	4.6	4.7	4.8	V
Current consumption		1.5	1.7	mA

Table 16. VCXO specification (continued)

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Output voltage	1.3	1.7	2.0	Vpp, sine wave for PLLs
Harmonics			–5	dBc
Control Voltage Range	0.25		4.45	V
Nominal Voltage for center frequency		2.2		V
Control Sensitivity	12	16	22	ppm/V
Frequency stability, vs. temperature vs. supply voltage vs. load vs. aging			 10 1 0.1 1	 ppm, –25...+70 deg.C ppm, 4.5 V +/– 5 % ppm, load +/– 10 % ppm, year
Operating temperature range	–20		70	deg. C
Load impedance: resistive part	2			kohm
parallel capacitance			20	pF

VHF PLL

The VHF PLL consists of the VHF VCO, PLL integrated circuit and loop filter. The output signal is used for the 2nd (and 3rd in PCN) mixer of the receiver and for the I/Q modulator of the transmitter.

Table 17. VHF PLL specification

Parameter	Minimum	Typical / Nominal		Maximum	Unit / Notes
Start up settling time				5	ms
Phase error				1	deg., rms
Sidebands		**GSM**	**PCN**		
+/– 200 kHz		–75	–75	–70	dBc
+/– 400 kHz		–84	–84	–70	dBc
+/– 1 MHz		<–85	–75	–70	dBc
+/– 2 MHz		<–85	<–80	–75	dBc
+/– 3 MHz		<–85	–85	–80	dBc
> 4 MHz		<–85	–85	–80	dBc

VHF VCO + buffer

The VHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and varactor diode as a resonance circuit. The buffer is combined into the VCO circuit so, that they use same collector current.

Table 18. VHF VCO + buffer specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.2	4.5	4.8	V
Control voltage	0.5		4.0	V
Supply current GSM PCN		2.5 3.5	5.0	mA mA
Operation frequency GSM PCN		232 400		MHz MHz
Output power level		170		mV_{rms} / 1 kohm
Control voltage sensitivity GSM PCN		 12 17		 MHz/V MHz/V
Phase noise, GSM/PCN f_0 +/– 25 kHz f_0 +/– 200 kHz f_0 +/– 1600 kHz f_0 +/– 3000 kHz			 –123 –133 –143	 dBc/Hz dBc/Hz dBc/Hz
Harmonics		–32	–30	dBc

UHF PLL

The UHF PLL consists of a UHF VCO, divider, PLL circuit and a loop filter. The output signal is used for the 1st mixer of the receiver and the upconversion mixer of the transmitter. In PCN the VCO changes the frequency according to the RX/TX mode change.

Table 19. UHF PLL specification

Parameter	Minimum	Typical / Nominal GSM	Typical / Nominal PCN	Maximum	Unit / Notes
Start up settling time				5	ms
Phase error				4	deg. rms
Settling time +/– 93 MHz GSM PCN		 525 450		800	µs µs µs
Sidebands offset from carrier +/– 200 kHz +/– 400 kHz +/– 600 kHz +/– 1.4 MHz...3.0 MHz > 3.0 MHz		 –80 –87 <–90 <–90	 –74 –81 <–90 <–90	 –60 –65 –70 –80 –80	 dBc dBc dBc dBc dBc

UHF VCO

The UHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and a varactor diode as a resonance circuit.

UHF VCO buffers

The UHF VCO output signal is divided into the 1st mixer of the receiver and the upconversion mixer of the transmitter. The UHF VCO signal is amplified after division. There is one buffer for TX and one for RX.

Table 20. UHF VCO buffer specification

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.2	4.5	4.8	V
Supply current		5.5	6.5	mA
Frequency range	See UHF VCO specification			MHz
Input power		–3		dBm
Harmonics			–10	dBc
Output amplitude		700		mVrms / 1 kohm

PLL Circuit

The PLL is Philips UMA1018 in GSM and National LMX2331 in PCN. The circuit is a dual frequency synthesizer including both the UHF and VHF synthesizers.

Table 21. PLL UMA1018 (UMA1020) specification

Parameter		Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage		2.7		5.5	V
Supply current	GSM PCN		8.5 12.1		mA mA
Principal input freq.	GSM PCN	500 200		1200 2000	MHz, Vdd = 4.5 V MHz, Vdd = 3.0 V
Auxiliary input freq.	GSM PCN	20 20		300 510	MHz, Vdd = 4.5 V MHz, Vdd = 3.0V
Input reference frequency		3		40	MHz, Vdd = 4.5 V
Input signal level	GSM PCN	50 –10 –15 500		500 4 4	mVrms dBm main divider dBm aux. divider mVrms ref. divider

Connections

Antenna

The default antenna in GSM transceiver is helix with turnable joint and in PCN a whip antenna with turnable joint also. The location of the antenna is in the gk2 module. The antenna signal is lead through the turnable hinge separating the gk2 and CMTmain modules using 50Ω flexible coaxial cable. The feedpoint of the antenna is matched to the 50Ω cable using LC matching transformer. There is a SMD coaxial connector on the CMT board for the cable.

Table 22. Specification of the antenna cable

Parameter		Minimum	Typical / Nominal	Maximum	Notes
Insertion loss	GSM PCN			0.6 dB 1.0 dB	Whole assembly including cable and connectors at both ends.
V.S.W.R.	GSM PCN			1.5 1.5	Whole assembly including cable and connectors at both ends.
Cable length			140 mm		

The external antenna connector includes an antenna switch between the built–in and external antennas. The nominal impedance of the external antenna connector is 50Ω. The connector is located near the duplex filter of the RF module

Chapter 4

–Transceiver GE8/GE9 – UIF Module

CONTENTS – User Interface

List of Figures

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Introduction

This document describe UIF (GK2 for GSM, GK2–1 for PCN) module. UIF module includes CMT display ,CMT keypad ,PDA soft keypad and antenna matching circuit with connectors. It has also connection to PDALCD (GK1). PDALCD and UIF modules, together these are called the LCDM. The LCDM has all the electronics in the cover side of RAE–1 (for GSM) and RAK–1 (for PCN).

Note: *GK2 is for GSM*
GK2–1 is for PCN

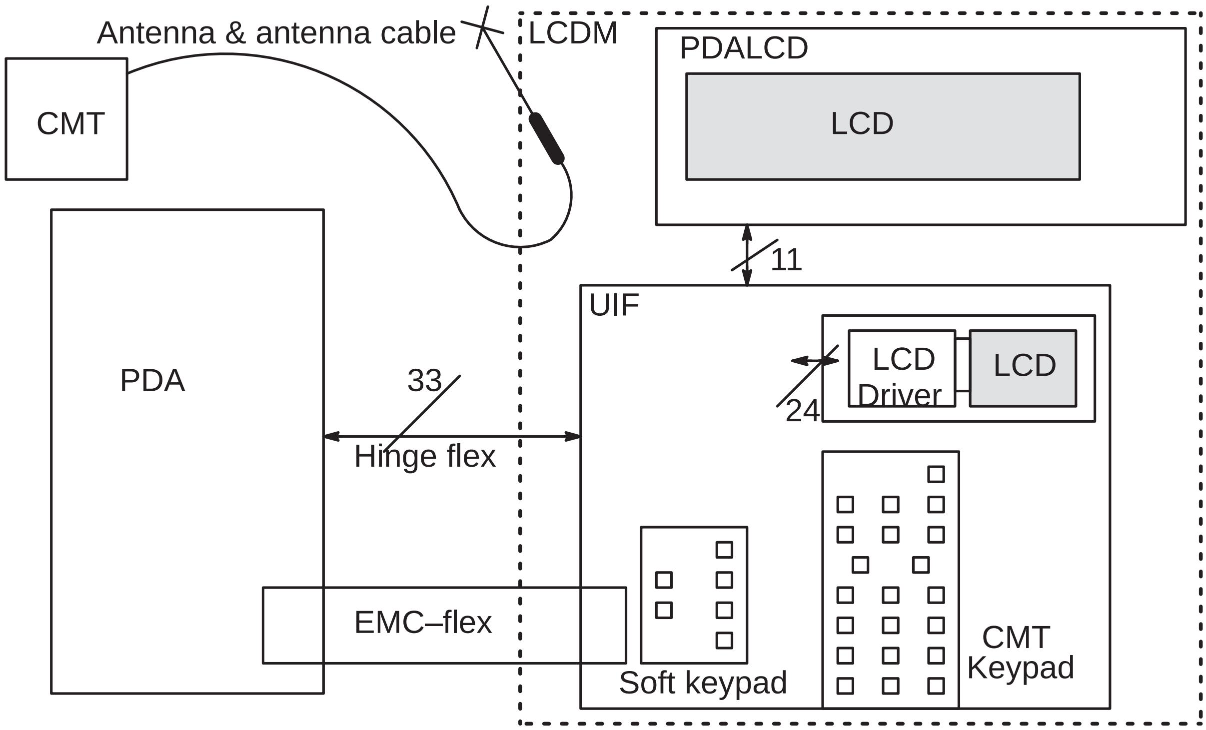

Figure 1. LCDM

Technical Summary

UIF Mechanics

The module is made for 0.6 mm thick Printed Circuit Board. PCB has four–layers. Reasons for that kind of material:

– Four layers are needed because of antenna is also assembled in this module. Additional layers will improve shielding against RF–radiation.

– We do not need Flexible Printed Circuit (As used in HD841) because we do not have side keys.

– PCB is easier to assembly than FPC.

– PCB is cheaper than FPC.

The major parts on the module assembly include the following:

– CMT Display module. Same module as used in HD841 including LCD, Heat seal, LCD driver TAB circuit and Light guide.
– CMT keydome assembly: Adhesive film holding 20 metal domes.
– Soft keys on the other side of PCB: four domes on the other end and two domes on the other end.
– 33–pin flex connector for hinge flex.
– 12–pin flex connector for GK1 display module.
– Coaxial cable connector for antenna cable.
– Antenna clips.
– 11 test pads.

Figure 2. shows the UIF mechanical shape and part placement.

Note: *For RAK –1 (GK2_1module) the antenna circuit is different from the one shown in this diagram. See the UIF Component Layout in section 10 for details.*

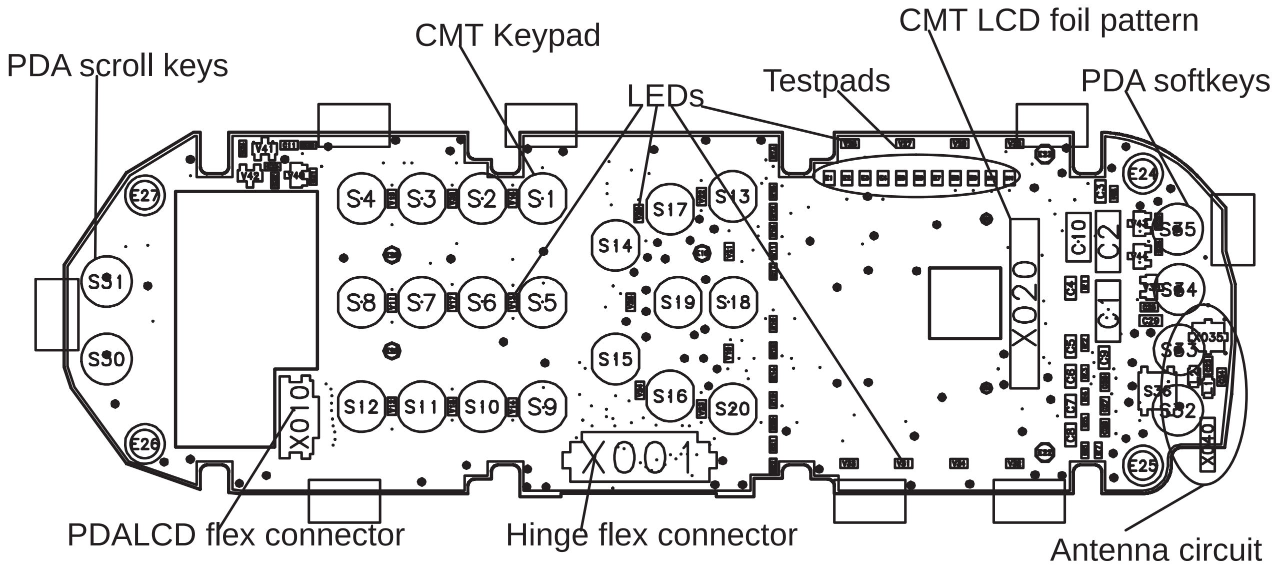

Figure 2. UIF Board

UIF Flexes

There is two flexes that are connected to the UIF module and go through the hinge. The other one is 33–pin flex. It has all active signals for the UIF module and three ground pins. It is connected to the 33–pin flex connector. The other one has one wide ground line. It is connected by using two sided copper tape with conducting adhesive. It is needed to improve EMC characteristics.

Both flexes are made of flexible material. Flexible material is needed because the hinge will be opened thousands of times and the signals must be working all the time.

UIF Electronics

The following sections of circuitry are on the UIF module:

– CMT LCD Display Module
– CMT LCD voltage divider & temperature compensation circuit.
– CMT Keypad & CMT LCD illuminating circuits.
– CMT & Soft keypad matrix.
– Antenna impedance matching circuit.
– Hinge flex connector.
– PDALCD flex connector.

Technical Specification

UIF Electrical Characteristics

DC Characteristics

Table 1. Supply Voltages and Power Consumption

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
2/X001	VL1	4.65	4.8	4.95	V
			1.5 mA		LCD material B
			0.8 mA		LCD material D (without temperature compensation)
1/X001	VBATT	5.3	7.2	8.4	V
			40 mA		Display illumination
			40 mA		Keypad illumination
27/X001	LCDVCC		3.3V		PDALCD Logic voltage
28/X001	LCDVEE	17V	22V	25V	PDALCD LCD voltage

Table 2. DC characteristics of PDA Hinge–flex connector on LCDM module

Pin / Type	Line Symbol	Mini-mum	Typi-cal / Nomi-nal	Maxi-mum	Notes	
10,17,24 / UIF	GND				GND	
6–3 / UIF	LCMUIF(3:0)	0V		0.7V	Output/Input low	keypad row lines/ display data lines
		4.65V	4.8V	4.95 V	Output/Input high	
7 / UIF	LCMUIF4	0V		0.7V	Output/Input low	keypad row read/write strobe for LCD driver
		4.65V	4.8V	4.95 V	Output/Input high	
8 / UIF	LCMUIF5	0V		0.7V	Output/Input low	keypad row LCD driver register select
		4.65V	4.8V	4.95 V	Output/Input high	
9 / UIF	LCMUIF6	0V		0.7V	Output/Input low	enable strobe for LCD driver
		4.65V	4.8V	4.95 V	Output/Input high	
14–11 / UIF	LCMCOL(3:0)	0V		0.7V	Output/Input low	Keypad column write
		4.65V	4.8V	4.95 V	Output/Input high	
15 / UIF	BACKLIGHTO	0V		0.7V	Output low, back-lights off	Display and key-pad illu-mination control
		4.65V	4.8V	4.95 V	Output high, back-lights on	
16 / UIF	LCMXPWRON	0V	0V	0.7V	Input low, power on/ off	Power ON/OFF key
			4.8V		Floating when inac-tive. A pull–up in PSL+.	
21–18 / PDALCD	LCDD(3:0)			0.4 V	Output low	PDA LCD, Data lines
		2.6 V			Output high	
22 / PDALCD	LP			0.4 V	Output low	PDA LCD, Line pulse
		2.6 V			Output high	
23 / PDALCD	PCLK			0.4 V	Output low	PDA LCD, Pixel clock
		2.6 V			Output high	

Table 2. DC characteristics of PDA Hinge–flex connector on LCDM module (continued)

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
25 / PDALCD	FP			0.4 V	Output low	PDA LCD, Frame Pulse
		2.6 V			Output high	
26 / PDALCD	DISPON			0.4 V	Output low	PDA Display on control signal
		2.6 V			Output high	
31–29 / UIF	KEYD(2:0)			0.4 V	Output low	Keymatrix drive lines
		2.6 V			Output high	Keymatrix drive lines
33, 32 / UIF	KEYS(1:0)	– 0.5 V		0.8 V	Input low	Keymatrix sense lines
		2.0 V		4.1 V	Input high	

AC Characteristics

Table 3. AC characteristics of RF connectors

Conn.	Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
X035, X040	Impedance		50		ohms
X035, X040	Transmitter frequency GSM PCN	 890 1710		 915 1785	 MHz MHz
X035, X040	Receiver frequency GSM PCN	 935 1805		 960 1880	 MHz MHz
X035, X040	Max. output power		2W (33 dBm) 1W (30 dBm)		GSM PCN

UIF External Signals and Connections

Table 4. Hinge flex connector (X001) signals

Signal Name	Pin	Signal description	Note
VBATT	1	Battery voltage	
VL1	2	CMT logic voltage	
LCMUIF(3:0)	6–3	keypad row / display data	
LCMUIF4	7	keypad row / Read/Write for strobe for CMT LCD	

Table 4. Hinge flex connector (X001) signals (continued)

Signal Name	Pin	Signal description	Note
LCMUIF5	8	keypad row / LCD driver register select	
LCMUIF6	9	enable strobe for LCD driver	
GND	10	Ground	
LCMCOL(3:0)	11–14	Keypad column write	
BACKLIGHTA	15	Display and keypad illumination control	
LCMXPWRON	16	CMT Power/Off key	
GND	17	Ground	
LCDD(3:0)	21–18	PDA LCD Data	
LP	22	PDA LCD Line Pulse	
PCLK	23	PCD LCD Pixel Clock	
GND	24	Ground	
FP	25	PDA LCD Frame Pulse	
DISPON	26	PDA Display ON Control signal	
LCDVCC	27	PDA LCD Logic voltage	
LCDVEE	28	PDA LCD Voltage	
KEYD(2:0)	31–29	PDA Keymatrix drive	
KEYS(1:0)	33–32	PDA Keymatrix sense lines	

Table 5. PDA LCD flex connector (X010) signals

Signal Name	Pin	Signal description	Note
Dispoff	1	Display On/Off signal	
FP	2	Frame Pulse	
LP	3	Line Pulse	
PCLK	4	Pixel Clock	
LCDD0	5	LCD Data	
LCDD1	6	LCD Data	
LCDD2	7	LCD Data	
LCDD3	8	LCD Data	
LCDVCC	9	LCD Logic Voltage	
GND	10,12	Ground	
LCDVEE	11	LCD Voltage	

Table 6. RF Connectors

Signal Name	Connector	Signal description	Note
RF1	X035	RF Signal to/from CMT module	
RF2	X040	RF Clips connector to/from Antenna	

UIF Mechanical Characteristics

Table 7. UIF Mechanical Characteristics

feature	value	notes
Weight	23g	Typical
Dimensions	165.0x50.8x4.0mm	Typical

Functional Description

UIF Circuit Description

The module is connected with 33 pin flex connector to the PDA Module, 24 pin soldered connection to the CMT LCD module and 12 pin connector to the PDALCD.

The module includes following main blocks:

– CMT keypad and PDA Soft keypad
– illumination
– CMT LCD Module interface
– PDA LCD connector
– Hinge flex connector
– Antenna impedance matching circuit
– Test pads for CMT LCD and LED testing
– Antenna connector and antenna clips

Keypad scanning and display driver control

COL(0–3) are used as column lines in keypad. UIF(0–5) are used as row lines. They are also multiplexed with display driver control signals.

When a key is pressed the ASIC gets an interrupt from a row and the MCU starts scanning. One column at a time is written to low and rows are used to read which key it was. The power off detection is multiplexed with one row; when all keys on the row seems to be pressed the ASIC knows that power key is pressed. The power key is also connected to PSL+ to switch the power on.

Row lines and UIF6 are used for display driver control. UIF(0–3) are used as 4 bit parallel data bus for the driver. UIF4 is used as read/write strobe, UIF5 to select data or instruction register and UIF6 as enable strobe.

Keypad and display illumination

The keypad illumination is achieved by using two transistors wired as simple constant current sinks. Each transistor supplies eight leds. The bases of the transistors are all wired together and supplied by emitter follower V40. The led current is fixed by the values of R33 and R34 and the ratio of R30 to R31. The current is about 5 mA/ each LED.

The display illumination operates in a similar way to the keypad drivers, two transistors are used to drive eight leds. The current in this case is defined by the value of R35, R36 and the ratio of R30 to R31. It is about 10 mA / each LED.

CMT LCD Module Interface

The LCD module includes the LCD and the display driver. The driver TAB is connected with heat seal connection to the LCD. The LCD is FSTN type. The duty ratio is 1/32 and the bias ratio 1/6.7. Viewing direction is 6 o‘clock.
The display driver is NJU6406–02 from JRC. It has internal clock oscillator and
negative voltage generator. It has 9600 bit character generator ROM and 64 * 8 bits character generator RAM. The display module is connected to the UIF module with 24 pin soldered connection.

The display module contains an oscillator to generate a negative voltage required for operation. The oscillator frequency is fixed on the UIF module by the resistance from pins 2 to 3 of X020, with the values of R6 and R7 shown, the frequency is within 180 kHz to 370 kHz. The negative going pulses appear at pin 9 of X020 where they are smoothed by C1 to give a voltage which is nominally equal but opposite to VL1.

For correct operation of the display, dc voltages between –VL1 and VL1 need to be generated and fed back to the driver chip, at pins 4 to 8 inclusive (of X020). The exact voltages depend on the relative values of the resistors R8, R1, R2, R3, R4 and R5.

The display driver is connected to the radio module with a 4 bit data bus. Data transfer is controlled with the following signals: R/W selects read or write operation (”0” = write, ”1” = read), Enable activates read/write operations and RS selects the register (”0” : instruction register (writing) or busy flag (reading), ”1” : data register).

PDA soft & scroll keys

Six PDA keys is located in the UIF module. They connected to the same keymatrix as other PDA keys.

Antenna matching circuit

The purpose of the antenna matching circuit is to transform the antenna feedpoint impedance to 50 ohm, which is the nominal impedance of the antenna cable. The matching circuit consists of a series inductor and capasitor and shunt inductor in GSM and series inductor and shunt inductor in PCN. The antenna matching circuit has its own ground area connected to the braid of the antenna cable. Antenna ground and digital ground are not connected together at the UIF Module.

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Chapter 5

– Transceiver GE8/GE9 – SIM Flex Module

CONTENTS – SIM flex

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List of Figures

Introduction

The purpose of the SIM–flex is basically to connect ancillary parts to the CMT. It has no active electronics and the main parts are the audio components, mic, low profile buzzer and speaker plus a SIM–connector.

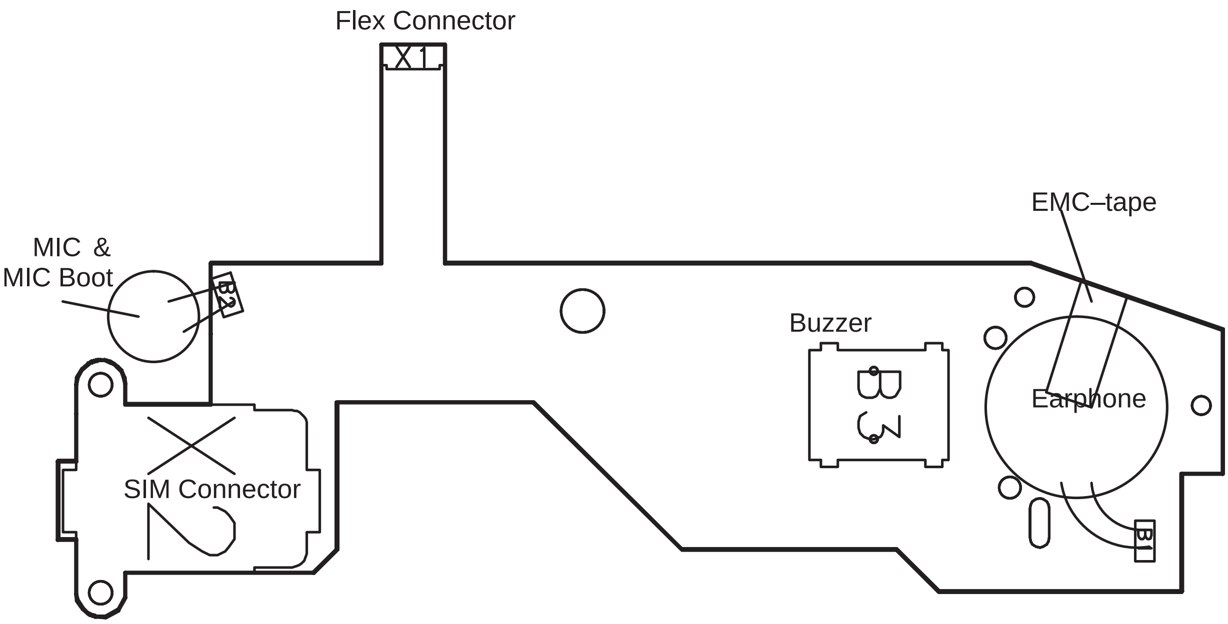

Figure 1. SIM Flex components.

Technical Specification

DC Characteristics

Table 1. Supply Voltages

Pin/ Connec-tor	Line Symbol	Mini-mum	Typi-cal / Nomi-nal (1)	Maxi-mum	Notes	
1 / SIM	BUZZ1	5.5V	7.2V	8.4V		
8 / SIM	VSIM	4.5V	4.8V	4.95V	SIM card reader supply voltage	

Table 2. Digital Control Signals

Pin/ Connec-tor	Line Symbol	Mini-mum	Typi-cal / Nomi-nal (1)	Maxi-mum	Notes	
2 / SIM	BUZZ2	0V		0.7V	Input low, buzzer on	
		5.5V	7.2V	8.4V	Input high, buzzer off	
6 / SIM	SIMCLK	3.6V	4.8V	4.95V	State ”1”	Clock for SIM card
		0V	0.2V	0.7V	State ”0”	
7 / SIM	SIMRESET	4.5V	4.8V	4.95V	Output high	Reset for SIM card
		0V		0.7V	Output low	
9 / SIM	SIMDATA	3.6V	4.8V	4.95V	State ”1”	Data for SIM card
		0V	0.2V	0.7V	State ”0”	

External Signals and Connections

Table 3. From CMT Module

Signal Name	Pin / Conn.	Notes
BUZZ1	1	Battery Voltage for buzzer
BUZZ2	2	PWM signal buzzer control
EARN	3	Earpiece (negative node)
EARP	4	Earpiece (positive node)
SIMCLK	6	Clock for SIM data
SIMRESET	7	Reset for SIM
SIMDATA	9	Serial data for SIM
VSIM	8	SIM supply voltage
GND	5, 10	Ground
MICP	12	Microphone (positive node)
MICN	11	Microphone (negative node)

Table 4. SIM Connector

Signal Name	Pin / Conn.	Notes
SIMCLK	1	Clock for SIM data
SIMRESET	2	Reset for SIM
SIMDATA	6	Serial data for SIM
VSIM	3, 5	SIM supply voltage
GND	4	Ground

AC Characteristics

Table 5. Audio Signals

Pin / Connector	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
12 / SIM 11 / SIM	MICP MICN		5 mV_{rms}	19 mV_{rms}	Differential
3 / SIM 4 / SIM	EARN EARP		124 mV_{rms}	1.965 V_{rms}	Differential, $R_L = 32\Omega$

Functional Description

Main Components

Audio components

The flex has three audio components: microphone, earphone and buzzer. Buzzer, mic and earphone are wired directly to flex connector without any extra components. Microphone has one capasitor that works as a RF filter.

Connectors

There is a custom design SIM Connector and flex connector shaped area in the flex.

Mecanical components

There is MIC Boot and EMC–tape for earpiece.

SIM interface

The SIM interface is the electrical interface between the smart card used in the GSM and PCN applications and the MCU via the ASIC. Four signals are used between the SIM card and the ASIC:

SIMDATA,

SIMCLK,

SIMRESET

VSIM.

Serial data is transferred between the card and the ASIC, the clock frequency is 3.25 MHz. When there is no data transfer between the SIM card and the CMT the clock can be reduced to 1.625 MHz. Some cards allow to stop the clock in that mode. The ASIC also generates the reset for the card and the supply voltage VSIM.

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Chapter 6

PDA Hardware Module GP1

CONTENTS – PDA unit

List of Figures

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Introduction

This chapter describes the PDA system hardware used in the NOKIA 9000 communicator. The PDA module is used to run all applications that utilise the bigger (640x200) LCD screen.

Technical Summary

Table 1. List of functional blocks on PDA module

Name of functional block	Function
PROCU	Execution and interface unit for PDA
PDAPWRU	Power supply unit
SIRU	Serial communication and Infrared Unit
EMIU	EMI supressing Unit

Most of the engine functionality is integrated on a chip that combines a CPU core and all needed peripherals; this chip and all other PDA module circuitry are mounted on a single multilayer printed circuit board. The chassis of the NOKIA 9000 communicator separates the CMT and PDA modules and also protects PDA circuits from EMI.

The components of the PDA system hardware are surface mounted soldered using reflow. The bottom connector (system connector) carries two optional through hole pins which might prove useful i.e., soldered by hand, if so required.

All PDA module components are located to one side of the PCB; the other side of the PCB is used for QWERTY keypad wiring matrix. The connection to the CMT module is made using a board to board connector and the connections from CMT to the phone User Interface module (UIF) are made through the PDA module. The connections to the PDALCD module and phone user interface module excluding audio, SIM card holder, buzzer, and call LED (UIF) are made using a flex cable.

The CMT module controls the battery charging via system connector on PDA. Test pads located to the PCB under the battery pack are for CMT flash loading and fieldtest purposes.

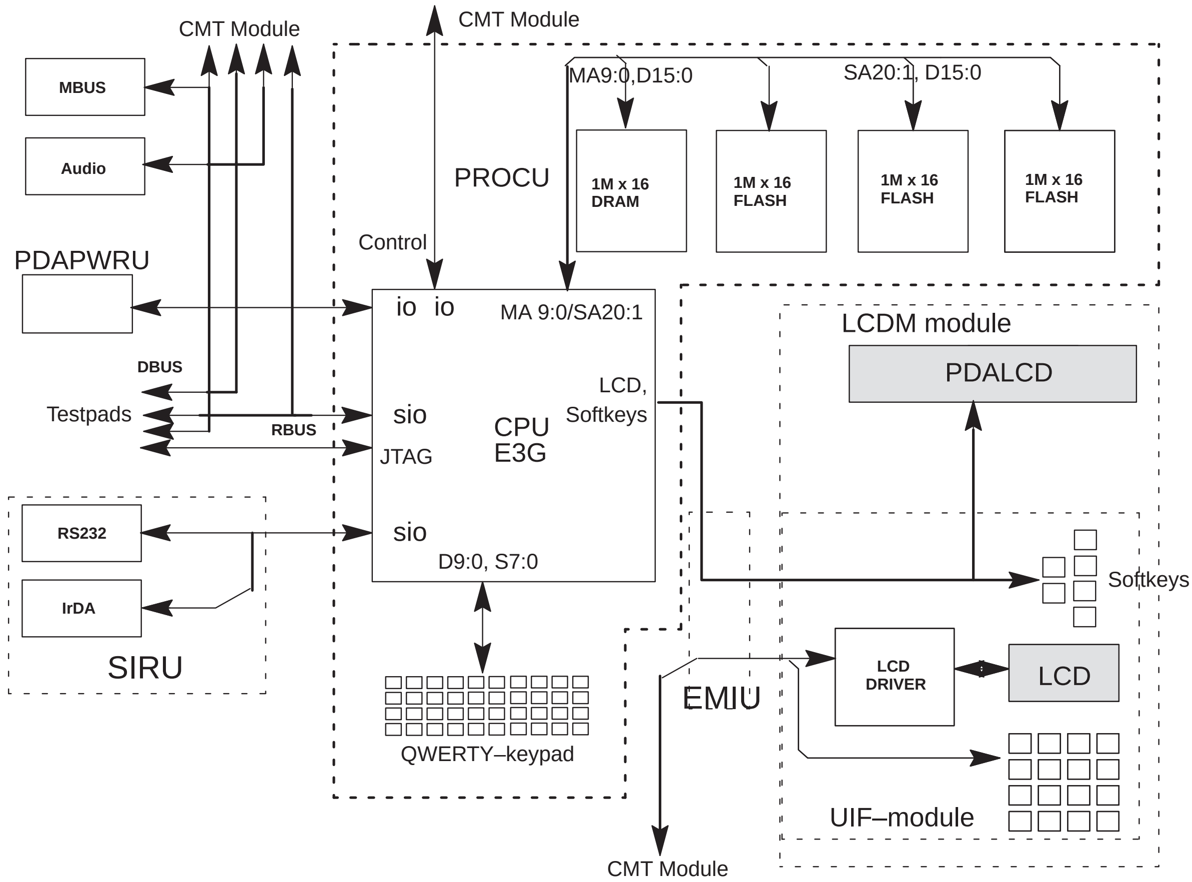

Figure 1. PDA Interconnection diagram

Modes of Operation

In principle there are four different operation modes

– fully on mode
– CPU core off mode (NAP)
– SUSPEND mode
– power supply off (Battery removed

The PDA module is always powered when a battery with adequate charge level is connected. Power saving in different modes is achieved by disabling clocks from functional blocks in an advanced manner. In the FULLY ON mode, all circuits are clocked, in the NAP mode, the CPU core is not clocked but all other circuits are clocked normally. In SUSPEND mode only the Real Time Clock (RTC) is clocked; DRAM is in self–refresh mode when the system is in SUSPEND mode. Asynchronous events, e.g., key presses and the lid being opened/closed, are able to wakeup the system from NAP and SUSPEND modes.

RTC is powered from the main battery as long as possible; in power supply OFF mode RTC is powered from the primary type of the backup battery.

DC Characteristics

Table 2. Supply Voltages and Power Consumption

Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
VB	5.75V	7.2V		CMT Software limit
	5.5V	7.2V	8.7 +/– 0.3V	CMT Hardware limit
	5.5V	7.2V	7.6 +/– 0.3V	CMT Hardware limit during a call
	4.9V	5.0V	5.1V	PDA Hardware limit
	5.9V	6.0V	6.1V	PDA Hardware limit cancel (remove VSYS shut-down)
VSYS	3.135V	3.3V	3.465V	regulator Imax=500mA
VCC5	4.825V	5.0V	5.175V	PDA FLASH programming voltage Imax=50mA
LCDVEE	17V	22V	25V	regulator Imax = 6mA PDALCD bias voltage
LCDVCC	3.135V	3.3V	3.465V	VSYS to LCD that can be switched off
VF (test)	11.4V	12V	12.6V	Flash programming voltage for CMT module
VL1	4.7V	4.85V	5.0V	CMT operating voltage
VCHAR	10.0V	12V	13.0V	Charger specification without load (PDA –> CMT)
VCHARGER	10.0V 730mA	12V 780mA	13.0V 830mA	Charger specification (VCHAR in to 9000)

Table 3. DC characteristics of board to board connector Signals

Pin / Type.	Line Symbol	Minimum	Typical / Nominal (1)	Maximum	Notes	
6 / UIF	BACKLIGHT	0V		0.7V	Output low, backlights off	Display and keypad illumination control
		4.7V	4.85V	5.0V	Output high, backlights on	
8 / PDA, test	RBUSRxD	2.735 V			State ”1”	RBUS received data to CMT
				0.4V	State ”0”	
		3.6V	4.85V	5.0V	State ”1”	RBUS received data to CMT (During CMT FLASH download
		0V	0.2V	0.7V	State ”0”	
9 / PDA, test	RBUSTxD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS transmitted data from CMT
		0V	0.2V	0.7V	State ”0”	
12 / UIF	XPWRON	0V	0V	0.7V	Input low, power on/off	
			4.65V		Floating when inactive. A pull–up in PSL+.	
15 / SIM	BUZZEROUT	0V		0.7V	Output low, buzzer off	
		5.2V	7.2V	8.4V	Output high, buzzer on	
20–17 / UIF	COL(3:0)	0V		0.7V	Input low	keypad columns
		4.7V	4.85V	5.0V	Input high	
27–24 / UIF	UIF(3:0)	0V		0.7V	Output/Input low	keypad row lines/ display data lines
		4.7V	4.85V	5.0V	Output/Input high	
28 / UIF	UIF4	0V		0.7V	Output/Input low	keypad row read/write strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	

Pin / Type.	Line Symbol	Mini-mum	Typi-cal / Nomi-nal (1)	Maxi-mum	Notes	
29 / UIF	UIF5	0V		0.7V	Output/Input low	keypad row LCD driver register select
		4.7V	4.85V	5.0V	Output/Input high	
30 / UIF	UIF6	0V		0.7V	Output/Input low	enable strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	
32 / test	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
33 / test	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
34 / test	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS re-ceived data to 9000
		0V	0.2V	0.7V	State ”0”	
35 / test	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS trans-mitted data from 9000
		0V	0.2V	0.7V	State ”0”	
36 / sys-tem, test	MBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/ s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
38 / PDA	LIDOPEN	2.735 V			State ”1”	Lid status for CMT module
				0.2V	State ”0”	

(1) Nominal voltage will be 4.75–5 V

Table 4. DC characteristics of system connector signals

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
1,2	VCHARGER	10V	12V	13.0 V	Isink < 730mA	Charger voltage
		730mA	800mA	870mA	Uin < 10V	
3	SYSMBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35 V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
4	TESTMODEX	2.0V		3.635 V	State ”1”	Test SW activation
		–0.5V		0.8V	State ”0”	
8	SYSTxD	5.0V	7.3V		Output high level	External serial data from Responder
			–7.3V	–5.0 V	Output low level	
9	SYSRxD	–25V		1.2V	Input low level	External serial data to responder
		2.4V		25V	Input high level	

Table 5. DC characteristics of signals on test pads under the battery pack

Pad	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
E100	JTAGTDI	2.0V		3.635 V	State ”1”	JTAG data in
		–0.5V		0.8V	State ”0”	
E101	JTAGTCK	2.0V		3.635 V	State ”1”	JTAG clock
		–0.5V		0.8V	State ”0”	
E102	JTAGTMS	2.0V		3.635 V	State ”1”	JTAG mode control
		–0.5V		0.8V	State ”0”	

Pad	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
E103	JTAGTDO	2.735 V			State ”1”	JTAG data out
				0.4V	State ”0”	
E104	MBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35 V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
E106	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
E107	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
E108	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS received data to HP
		0V	0.2V	0.7V	State ”0”	
E109	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS transmitted data from HP
		0V	0.2V	0.7V	State ”0”	
8 / PDA, test	RBUSRxD	2.735 V			State ”1”	RBUS received data to CMT
				0.4V	State ”0”	
		3.6V	4.85V	5.0V	State ”1”	RBUS received data to CMT (During CMT FLASH download
		0V	0.2V	0.7V	State ”0”	
E112	RBUSTxD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS transmitted data from CMT
		0V	0.2V	0.7V	State ”0”	
E113	TESTMODEX	2.0V		3.635 V	State ”1”	Test SW activation
		–0.5V		0.8V	State ”0”	

Table 6. DC characteristics of LCDM flex connector on PDA module

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
6–3 / UIF	LCMUIF(3:0)	0V		0.7V	Output/Input low	keypad row lines/ display data lines
		4.65V		4.95V	Output/Input high	
7 / UIF	LCMUIF4	0V		0.7V	Output/Input low	keypad row read/write strobe for LCD driver
		4.65V		4.95V	Output/Input high	
8 / UIF	LCMUIF5	0V		0.7V	Output/Input low	keypad row LCD driver register select
		4.65V		4.95V	Output/Input high	
9 / UIF	LCMUIF6	0V		0.7V	Output/Input low	enable strobe for LCD driver
		4.65V		4.95V	Output/Input high	
14–11 / UIF	LCMCOL(3:0)	0V		0.7V	Output/Input low	Keypad column write
		4.65V		4.95V	Output/Input high	
15 / UIF	BACKLIGHTO	0V		0.7V	Output low, backlights off	Display and keypad illumination control
		4.65V	4.80V	4.95V	Output high, backlights on	
16 / UIF	LCMXPRON	0V	0V	0.7V	Input low, power on/off	Power ON/OFF key
			4.65V		Floating when inactive. A pull–up in PSL+.	
21–18 / PDALCD	LCDD(3:0)			0.4 V	Output low	PDA LCD, Data lines
		2.735 V			Output high	
22 / PDALCD	LP			0.4 V	Output low	PDA LCD, Line pulse
		2.735 V			Output high	
23 / PDALCD	PCLK			0.4 V	Output low	PDA LCD, Pixel clock
		2.735 V			Output high	

Table 6. DC characteristics of LCDM flex connector on PDA module (continued)

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
25 / PDALCD	FP			0.4 V	Output low	PDA LCD, Frame Pulse
		2.735 V			Output high	
26 / PDALCD	DISPON			0.4 V	Output low	PDA Display on control signal
		2.735 V			Output high	
31–29 / UIF	KEYD(2:0)			0.4 V	Output low	Keymatrix drive lines
		2.735 V			Output high	
33, 32 / UIF	KEYS(1:0)	– 0.5 V		0.8 V	Input low	Keymatrix sense lines
		2.0 V		3.635 V	Input high	

AC Characteristics

Table 7. Audio Signals

Pin / Type (1, 2)	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	
42 / B2B	EXTEAR		130 mV_{rms}	500 mV_{rms}	
41 / SC	SYSEXTMIC		200 mV_{rms}	530 mV_{rms}	
42 / SC	SYSEXTEAR		130 mV_{rms}	500 mV_{rms}	

Note 1. B2B = Board to board connector between PDA and CMT modules
Note 2. SC = System Connector

Connectors

Connectors Inside Transceiver Unit

Table 8. PDA board to board connector

Signal Name	Pin	Notes
VB	1, 44	Battery voltage
GND	2, 5, 7, 10, 13, 21, 22, 23, 37, 39, 40	Ground
PHFMICN	3	PHF microphone (negative node)
PHFMICP	4	PHF microphone (positive node)
BACKLIGHT	6	Backlights on/off
RBUSRxD	8	RBUS receive (CMT <– PDA or test)
RBUSTxD	9	RBUS transmit (CMT –> PDA or test)
VL1	11	Logic supply voltage (4.75–5V)
XPWRON	12	Power key (active low)
VCHAR	14,31	Battery charging voltage. 2 pins needed
BUZZEROUT	15	Buzzer signal to buzzer on SIM module
VF	16	Programming voltage for flash.
COL(3:0)	20–17	Lines for keypad write
UIF(3:0)	27–24	Lines for keypad read and LCD–controller data
UIF4	28	Line for keypad read and LCD–controller read/ write strobe
UIF5	29	Line for keypad read and LCD–controller data/ instruction register selection
UIF6	30	LCD–controller enable strobe
DCLK	32	DBUS–data clock
DSYNC	33	DBUS–data bit sync clock
RDA	34	DBUS received data from the accessories
TDA	35	DBUS transmit data to the accessories
MBUS	36	Serial bidirectional data and control between the handphone and accessories.
LIDOPEN	38	Lid status for CMT module

Table 8. PDA board to board connector (continued)

Signal Name	Pin	Notes
EXTMIC	41	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
EXTEAR	42	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
AGND	43	Analog ground for accessories. Connected directly to digital ground on the PCB.

Table 9. HFMIC Connector

Signal Name	Pin	Notes
PHFMICN	1	Negative MIC input
PHFMICP	2	Positive MIC input

Table 10. LCDM module flex connector on PROCU

Signal Name	Pin	Notes
GND	10, 17, 24	Ground or VB (flex material dependent)
VB	1	Power lines for backlight LEDs
VL1	2	Phone LCD power
LCMUIF(3:0)	6, 5, 4, 3	Lines for keypad read and LCD–controller data
LCMUIF4	7	Line for keypad read and LCD–controller read/ write strobe
LCMUIF5	8	Line for keypad read and LCD–controller data/ instruction register selection
LCMUIF6	9	LCD–controller enable strobe
LCMCOL(3:0)	14, 13, 12, 11	Lines for keypad write
BACKLIGHTO	15	Backlights on/off (controll)
LCMXPRON	16	Power ON/OFF key
LCDD(3:0)	21, 20, 19, 18	PDA LCD Data lines
LP	22	PDA LCD, Line pulse
PCLK	23	PDA LCD, Pixel clock
FP	25	PDA LCD, Frame Pulse
DISPON	26	PDA Display on control signal
LCDVCC	27	PDA LCD Logic voltage
LCDVEE	28	PDA LCD Bias voltage (+21V)
KEYD(2:0)	31, 30, 29	Keymatrix drive lines
KEYS(1:0)	33, 32	Keymatrix sense lines

Connectors Out of Transceiver Unit

Table 11. System Connector

Signal Name	Pin	Notes
VCHARGER	1, 2	Battery charging voltage.
SYSMBUS	3	Serial bidirectional data and control between the handphone and accessories.
TESTMODEX	4	Test SW activation
SYSEXTMIC	6	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
SYSEXTEAR	7	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
SYSTXD	8	External serial data from the 9000
SYSRXD	9	External serial data to 9000
AGND	10	Analog ground for accessories. Connected directly to digital ground on the PCB.
GND	5, 11, 12	Charger and digital ground.

Table 12. Test pads under the battery pack

Signal Name	Pad	Notes
JTAGTDI	E100	JTAG data in
JTAGTCK	E101	JTAG clock
JTAGTMS	E102	JTAG mode control
JTAGTDO	E103	JTAG data out
MBUS	E104	Serial bidirectional data and control between the handphone and accessories.
VF	E105	Flash programming voltage
DCLK	E106	DBUS–data clock
DSYNC	E107	DBUS–data bit sync clock
RDA	E108	DBUS received data from the accessories
TDA	E109	DBUS transmit data to the accessories
GND	E110	Signal ground
RBUSRxD	E111	RBUS receive (CMT <– PDA or test)
RBUSTxD	E112	RBUS transmit (CMT –> PDA or test)
TESTMODEX	E113	PDA test SW activation

Internal Signals and Connections

Table 13. Signals Between PROCU and power supply unit

Signal Name	Function	Notes
LCDPWM	PWM signal for LCD voltage control	LCD contrast control
LCDVCCON	LCD Vcc on/off	
LCDVEEON	LCD Vee on/off	
PWRGOOD	Reset signal for CPU	VSYS valid
VBACK	Backup battery voltage to RTC	
5VPDX	5V regulator powerdown	

Functional Description

Introduction

Intel E3G is 386 based core with all needed peripherals on same chip. E3G is used to execute all applications, GEOS, DOS, BIOS, and TFFS.

Clocking Scheme

Actual clock signals are not routed to any other chip than previously mentioned E3G. All clocks are generated from a 32.768 kHz chrystal with PLL's integrated to the E3G CPU chip.
System clock rates are as follows:

CPU core	23.96 MHz
UART's	1.84MHz
8254 Timer	1.198MHz
RTC	32.768kHz

Reset and Power Management

Power good (PWRGOOD) signal from PDAPWRU module is used as a system reset. Both PDA and CMT modules power management system is implemented with special hardware in close co–operation with operating system.

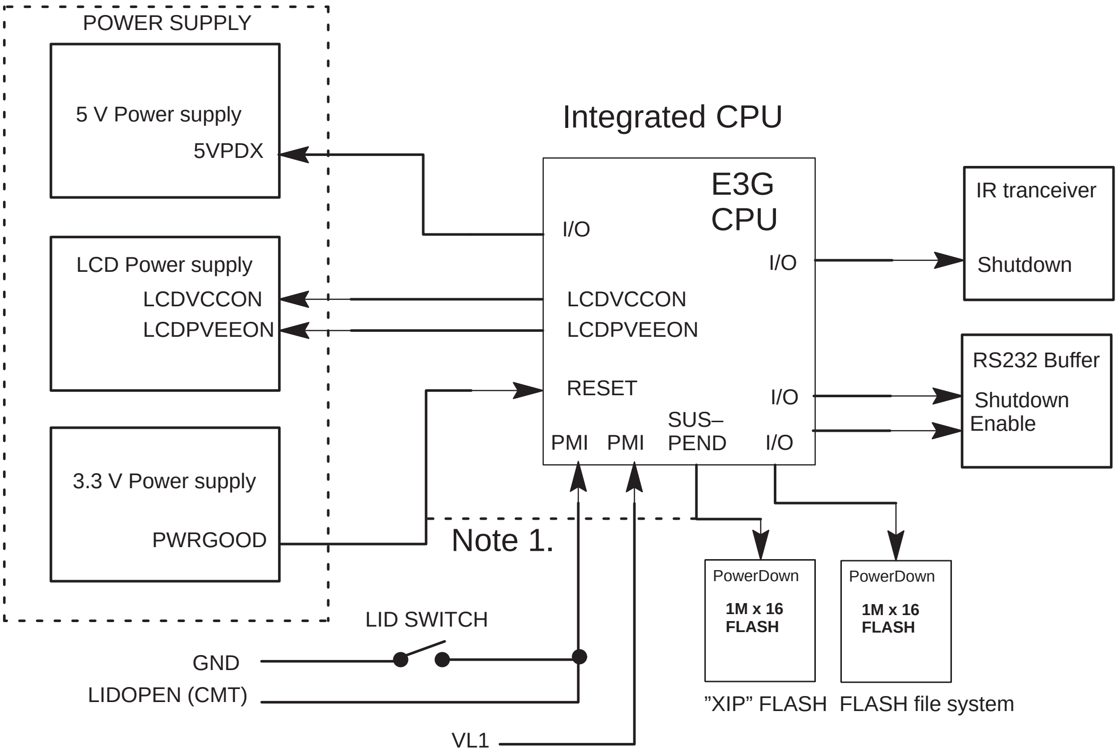

Figure 2. Reset and power management block diagram

PDA power management principle.

Operating voltage is always ON on the PDA module when battery is connected and charge level on the battery is above PDA power supply limit (HW cutt–off). When battery is connected voltage must rise over 'PDA HW limit cancel voltage' to start CPU power–up. Power consumption reduction is achieved by stopping clocks from the system (stable state power consumption in CMOS logic is really small).
From CMT point of view PDA module have only two states PDA_ON and PDA_SUSPEND illustrated in figure 3. When PDA is in PDA_SUSPEND state it takes about 500 ms (max) Note 1. to wake it up. During the wakeup period all messages from CMT are discarded. When PDA is in PDA_ON it wakes up immediately (max few microseconds) and messages are not discarded. CMT is never able to be ON when PDA is not able to wakeup because CMT is switched OFF before PDA when battery level is falling. See Figure 5 that depicts battery charge levels and its effects to PDA and CMT modules.

Note 1. On A–3 CPU version startup time in low temperatures is up to 20s

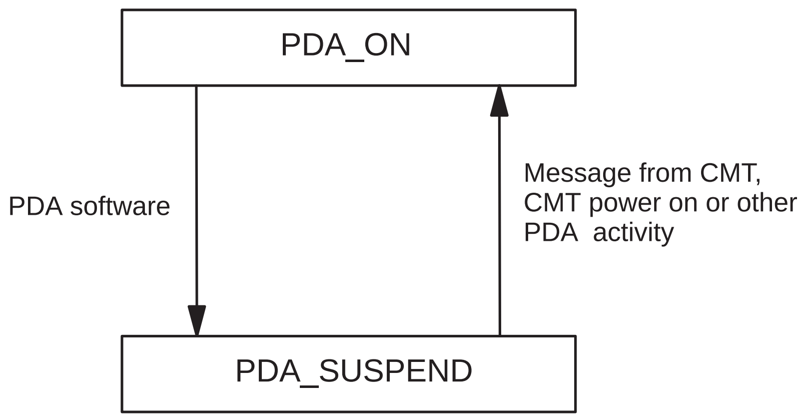

Figure 3. PDA power states from CMT point of view.

The PDA knows whether CMT is on or off by monitoring VL1. It gets information about battery level by asking for battery level from the CMT.

The PDA is able to switch CMT to the CMT_PDA_REQUEST_SERVICE state.

CMT power management principle.

The goal is that existing power management scheme of CMT in HD841 is changed as little as possible. CMT module has power switch that works as on normal DCT1 cellular phones. The CMT_PDA_REQUEST_SERVICE state is implemented to support requests from PDA even when CMT is switched off. RF is not activated when CMT is on the CMT_PDA_REQUEST_SERVICE state. If CMT_PDA_REQUEST_SERVICE state is activated by PDA, CMT switches itself off after requested action is done. CMT power states are illustrated in Figure 4.

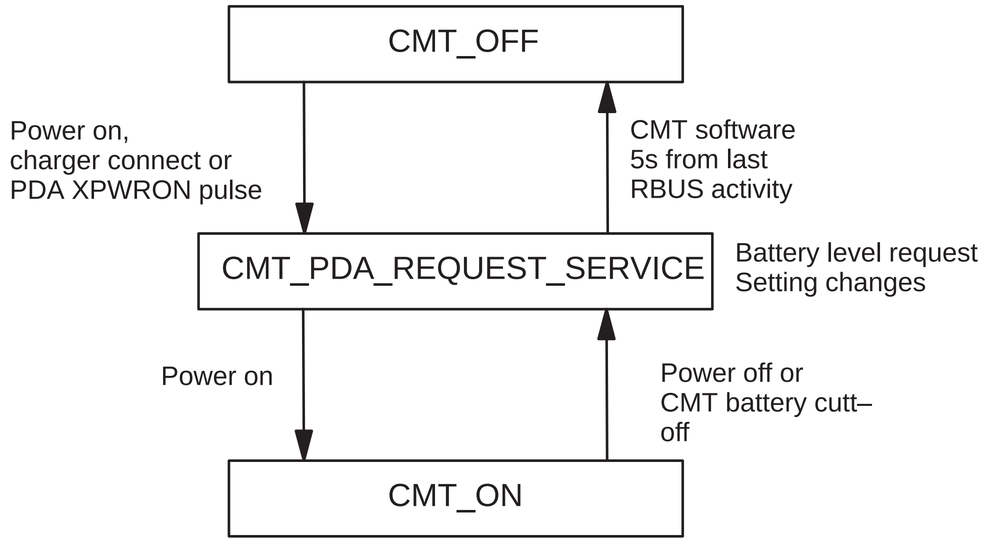

Figure 4. CMT power states from PDA point of view.

Battery charge level limits on CMT and PDA

Figure 5 (overleaf) shows an example of combined CMT and PDA critical battery levels, measurement accuracy (+/– 50mV). There are two kind of limits most of which are implemented in software.

The AD converter, located in the CMT module, is used as a source for battery level values needed by both CMT and PDA software. PDA gets battery level information from the AD converter via ECI messages. The CMT HW limit, PDA HW cut–off and Battery protect circuit cut–off are implemented in hardware and actions are taken without notice to any software.

The following limits are based on battery level values read from the AD converter; decisions are made by software.

- *Battery low level warning 1*
  If CMT is ON this warning is generated by CMT sending a message to PDA when warning 1 is triggered. If CMT is OFF, PDA must generate this warning itself.
- *CMT battery cut–off*
  CMT switches itself off when battery level has fallen below this level.
- *Battery low level warning 2*
  PDA generates this warning when the battery level value read from CMT has fallen below this level.
- *PDA limit (Data save)*
  PDA saves all user data and disables PDA when the battery level is below this level.

The following limits are implemented in hardware:

- *CMT HW limit*
  CMT power supply switches itself off.
- *PDA HW cut–off*
  PDA power supply switches itself off.
- *Battery protect circuit cut–off*
  A circuit in the battery package switches power off from battery output pads.

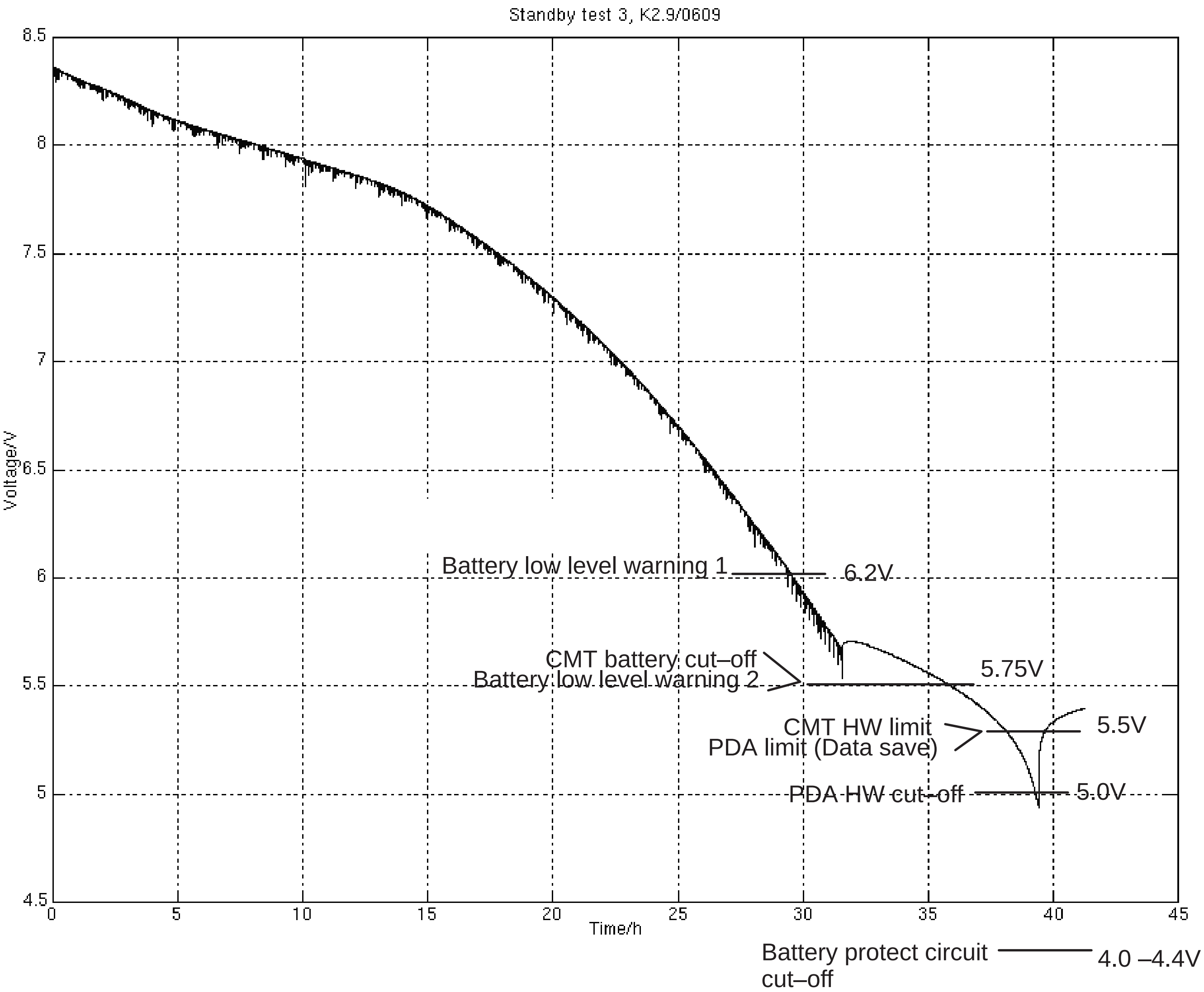

Figure 5. Discharge voltage curve of battery (two Li–Ion cells) in stadby

EMIU

This module contains only passive components to suppress EMI generated voltages on external signal lines.

Note 1. B2B = Board to board connector between PDA and CMT modules

Table 14. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
BACKLIGHTI	Backlights on/off (control)	B2B / Back-light
KEYDI(2:0)	Keymatrix drive lines	PROCU / KEYD(2:0)
KEYSI(1:0)	Keymatrix sense lines	PROCU / KEYS(1:0)
LCDD(3:0)	PDA LCD Data	PROCU / LCDD(3:0)
DISPONI	PDA LCD Display on control signal	PROCU / DISPON
FPI	PDA LCD Frame Pulse	PROCU / FP
PCLKI	PDA LCD Pixel Clock	PROCU / PCLK
LPI	PDA LCD Line Pulse	PROCU / LP
PHFMICNI	Negative Hands Free MIC input	B2B / PHFMICN
PHFMICPI	Positive Hands Free MIC input	B2B / PHFMICP
COL(3:0)I	Lines for keypad write	B2B / COL(3:0)
UIF(3:0)I	Lines for keypad read and LCD–controller data	B2B / UIF(3:0)
UIF4I	Line for keypad read and LCD–controller read/write strobe	B2B / UIF4
UIF5I	Line for keypad read and LCD–controller data/insruction register selection	B2B / UIF5
UIF6I	LCD–controller enable srobe	B2B / UIF6
MBUSI	Serial bidirectional data and control between the handphone and accesseries	B2B / MBUS
EXTMICI	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT	B2B / EX-TMIC
EXTEARI	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.	B2B / EX-TEAR

Note 1. LCMCON = LCD module connector on PDA module

Note 2. MICCON = Hands–free microfone connector on PDA module
Note 3. SC = System Connector

Table 15. External Signals and Connections, Outputs

Signal Name	Signal description	To (1,2,3)
BACKLIGHTO	Backlights on/off (control)	LCDMCON / BACKLIGH-TO
KEYDO(2:0)	Keymatrix drive lines	LCMCON / KEYD(2:0)
KEYSO(1:0)	Keymatrix sense lines	LCMCON / KEYS(1:0)
LCDDO(3:0)	PDA LCD Data	LCMCON / LCDD(3:0)
DISPONO	PDA LCD Display on control signal	LCMCON / DISPON
FPO	PDA LCD Frame Pulse	LCMCON / FP
PCLKO	PDA LCD Pixel Clock	LCMCON / PCLK
LPO	PDA LCD Line Pulse	LCMCON / LP
PHFMICNO	Negative Hands Free MIC input	MICCON / 1
PHFMICPO	Positive Hands Free MIC input	MICCON / 2
COL(3:0)O	Lines for keypad write	LCDMCON / LCDMCOL(3:0)
UIF(3:0)O	Lines for keypad read and LCD–controller data	LCDMCON / LCDMUIF(3:0)
UIF4O	Line for keypad read and LCD–controller read/write strobe	LCDMCON / LCDMUIF4
UIF5O	Line for keypad read and LCD–controller data/insruction register selection	LCDMCON / LCDMUIF5
UIF6O	LCD–controller enable srobe	LCDMCON / LCDMUIF6
MBUSO	Serial bidirectional data and control between the handphone and accesseries	SC / SYSM-BUS
EXTMICO	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in HP	SC / SY-SEXTMIC
EXTEARO	External audio output to accessories or handsfree speaker. 100kΩ pull–down in HP to turn on the junction box.	SC / SY-SEXTEAR

PROCU

The Processing unit contains integrated Intel E3G CPU (CPU and peripherals on the same chip), two types of memory circuits (DRAM, FLASH), a 22–bit address bus (26 bit internally), and a 16–bit data bus.

PROCU functions:

– GEOS, DOS, BIOS, TFFS and GEOS application platform
– user interface functions
– external interfaces (IrDA and RS232)
– power management
– self–test, production testing, and maintenance

Technical specifications

Table 16. External Signals and Connections, Inputs

Signal Name	Signal description	From
VSYS	System voltage 3.3V	PDAPWRU
VCC5	5V for FLASH and RBUS	PDAPWRU
VB	Battery voltage	B2B / VB
VL1	CMT operating voltage	B2B / VL1
PWRGOOD	Reset signal for CPU	PDAPWRU
VBACK	Backup battery voltage to RTC	PDAPWRU
RBUSTXD	RBUS transmit of CMT	B2B / RBUSTXD
RSRXD	Serial data to PDA module	SIRU
TESTMODEX	PDA test SW activation	Test pad / E113
JTAGTDI	JTAG data in	Test pad / E100
JTAGTCK	JTAG clock	Test pad / E101
JTAGTMS	JTAG mode control	Test pad / E102
KEYS(1:0)	Keymatrix sense lines	EMIU

Table 17. External Signals and Connections, Outputs

Signal Name	Signal description	To
LIDOPEN	Lid status for CMT module	B2B / LIDO-PEN
LCDVCCON	LCD Vcc on/off	PDAPWRU
LCDVEEON	LCD Vee on/off	PDAPWRU
LCDPWM	PWM signal for LCD voltage control	PDAPWRU

Table 17. External Signals and Connections, Outputs (continued)

Signal Name	Signal description	To
5VPDX	5V regulator powerdown	PDAPWRU
XPWRON	Power key (active low)	B2B / XPOWER-ON, LCMCON / LCMXPOW-ERON
RBUSRXD	RBUS receive of CMT (CMT <– PDA)	B2B / RBUSRXD
RSTXD	Serial data from PROCU module	SIRU
RSENX	RS buffer enable	SIRU
RSSHDX	RS buffer shutdown	SIRU
IRSHD	IR tranceiver shutdown	SIRU
JTAGTDO	JTAG data out	Test pad E103
BUZZEROUT	Buzzer signal to buzzer on SIM module	B2B / BUZZER-OUT
LP	PDA LCD Line Pulse	EMIU
PCLK	PDA LCD Pixel Clock	EMIU
FP	PDA LCD Frame Pulse	EMIU
LCDD(3:0)	PDA LCD Data	EMIU
DISPON	PDA display on control signal	EMIU
KEYD(2:0)	Keymatrix drive lines	EMIU

Block description

– PROCU Memories

Two types of memory is used: DRAM, and FLASH (ROM). The E3G CPU has a 22 bits (26 bit internal) wide external address bus A(21:0) and an 16–bit data bus. The address bits A(25:11) are used for chip select decoding. The decoding is done internally on the E3G CPU.

PROCU memory map is illustrated in figures 1 and 2 and in Table 31

DRAM (70 ns) is refreshed only when main battery is connected. As long as the main battery has power and is connected all the DRAM data stays valid. When the main battery is removed all the DRAM data is lost.

All application data is saved to nonvolatile FLASH memory under control of flash file system (TFFS by M–Systems). Application status is not stored.

DRAM area is composed of a single 1M x 16 bit chip. The access time of 70 ns enables zero wait–state page access and one wait–state page fault.

FLASH memory is used for two purposes on this device. Two 1M x 16 bit chips (75 ns) are used for BIOS, DOS, GEOS and applications this memory is usually called XIP FLASH. A 1M x 16 bit chip (120 ns) is used to save user data. This memory device is handled by FLASH file system. From application point of view this memory is accessed like hard disk using INT13 functions. 75 ns FLASH device needs one wait–state and 120 ns device two wait–states.

FLASH devices are equipped with Reset/Power down pin (RP#) which can be used to place devices in a Deep PowerDown state. RP# pin of two XIP FLASH devices is connected to SUSPEND pin of E3G. SUSPEND# pin is active when E3G is in SUSPEND mode and internal PLL's are not runnig. RP# pin of the FLASH device under TFFS is connected to a GPIO pin and it is controlled by TFFS. TFFS and RS232 flash download softwares are able to control 5V power supply powerdown. There is 100us delay needed between 5V power up and write command.

1 Mbyte of address space is directly addressable by the CPU (conventional memory). Any additional memory is accessed via Expanded Memory System EMS . EMS system follows LIM 4.0 specification.

Memory Map

Table 18. Memory Map

000000 00FFFF	Interrupt Vector, DOS data (DRAM)
010000 07FFFF	GEOS heap (DRAM)
09E400 0A03FF	True FFS data (DRAM)
0A0400 0A05FF	BIOS data (DRAM)
0A0600 0AFFFF	Video buffer (DRAM)
0B0000 0B3FFF	EMS page 0 (True FFS & GEOS ROM disk)
0B4000 0B7FFF	EMS page 1 (XIP page 2) EMS register

Table 18. (continued) Memory Map

0B8000 0B2BFFF	EMS page 2 (XIP page 1) EMS register
0BC000 0BFFFF	EMS page 3 (Fixed GEOS XIP) EMS register
0C0000 0ECBFF	GEOS XIP (XIP FLASH 1.) Double mapped area
0ECC00 0F77FF	ROM–DOS (XIP FLASH 1.) Double mapped area
0F7000 0FBFFF	True FFS (XIP FLASH 1.) Double mapped area
0FC000 0FFFFF	BIOS (XIP FLASH 1.) Double mapped area
100000 1FFFFF	SWAP/RAMDISK (Uppermost meg of DRAM)
200000 24FFFF	SWAP/RAMDISK (DRAM Roll–Over. The DRAM area that is ”under” double mapped XIP FLASH and EMS registers.)
3A00000 3BFFFFF	True FFS FLASH area
3C00000 3DFFFFF	GEOS and applications (XIP FLASH 2)
3E00000 3EBFFFF	GEOS and applications (XIP FLASH 1)
3EC0000 3EECBFF	GEOS XIP (XIP FLASH 1)
3EECC00 3EF77FF	ROM–DOS (XIP FLASH 1)
3EF7800 3EFC7FF	True FFS (XIP FLASH 1)
3EFC800 3EFFFFF	BIOS (XIP FLASH 1)

Table 18. (continued) Memory Map

3F00000 3FFFBFF	DOS ROM–DISK about 80k GEOS and applications (XIP FLASH 1) Upper non–resident XIP
3FFFC00 3FFFF9F	Reserved for manufacturing and aftersales data
3FFFFA0 3FFFFAF	PDA_PROD_HW_VERSION
3FFFFB0 3FFFFBF	PDA_PROD_HW_CODE
3FFFFC0 3FFFFCF	PDA_PROD_HW_NUMBER
3FFFFD0 3FFFFEF	PDA_SW VERSION
3FFFFF0 3FFFFFB	Jump to BIOS code jump command
3FFFFFC 3FFFFFF	Image checksum

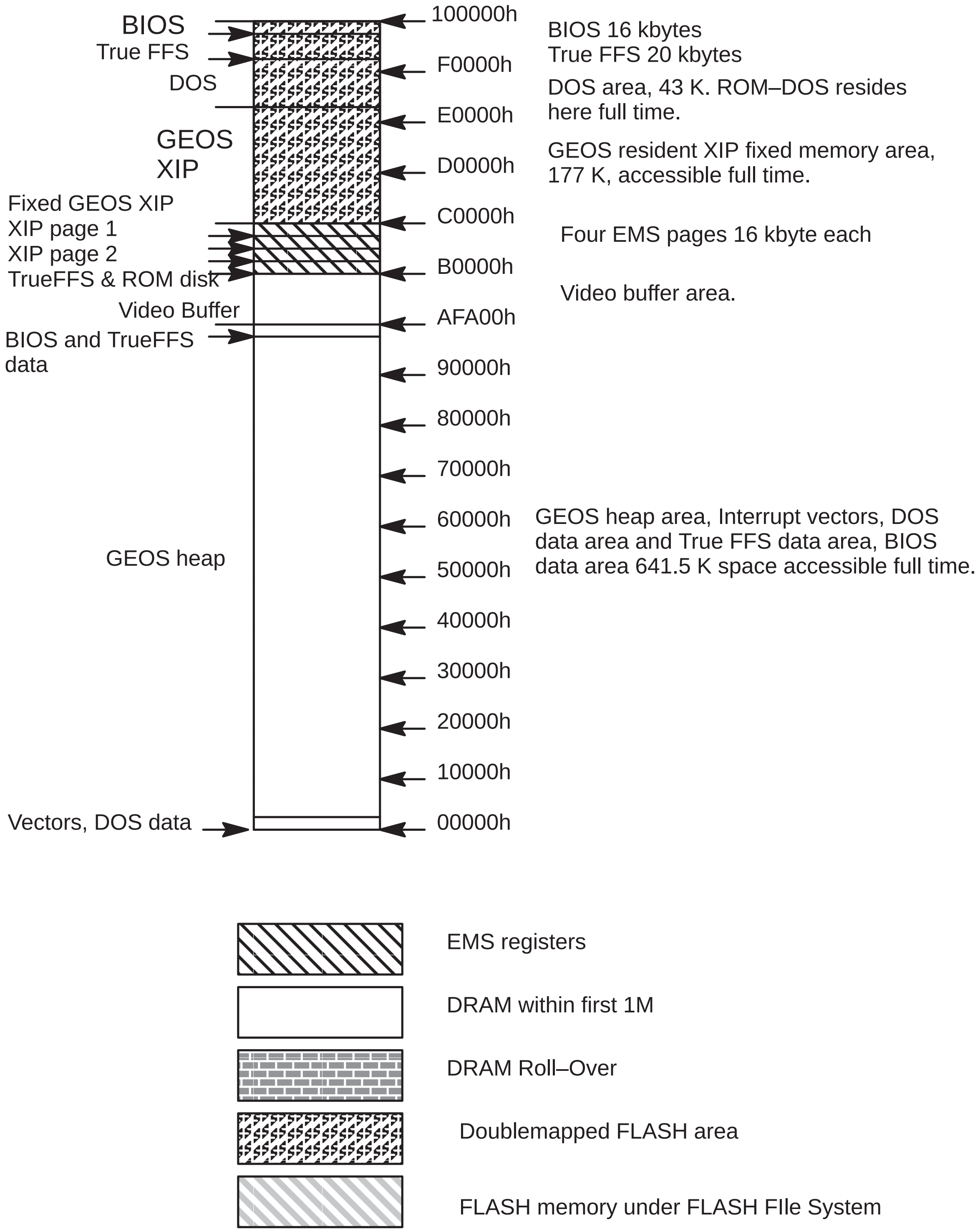

Figure 6. PROCU memory map part 1

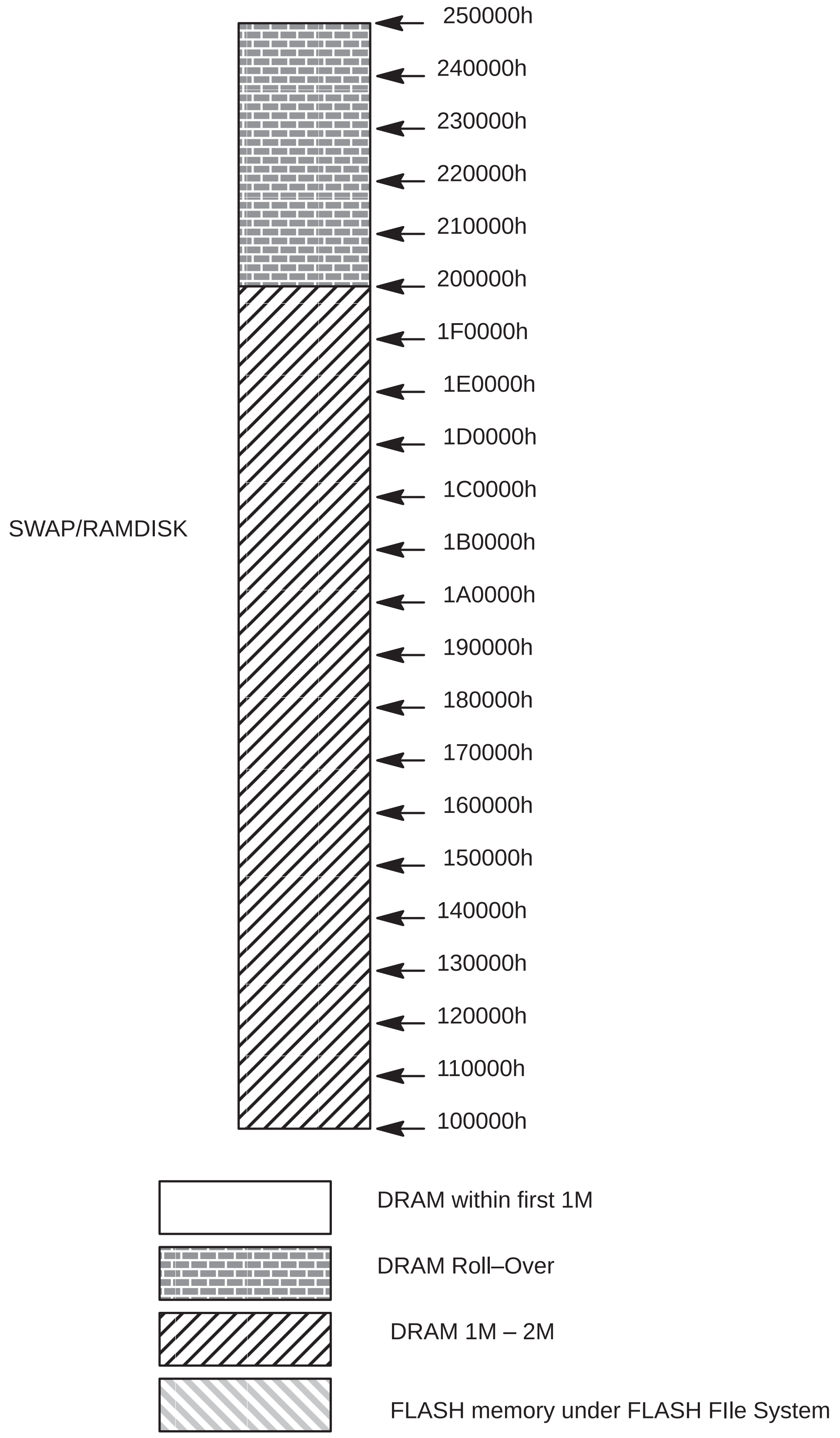

Figure 7. PROCU memory map part 2

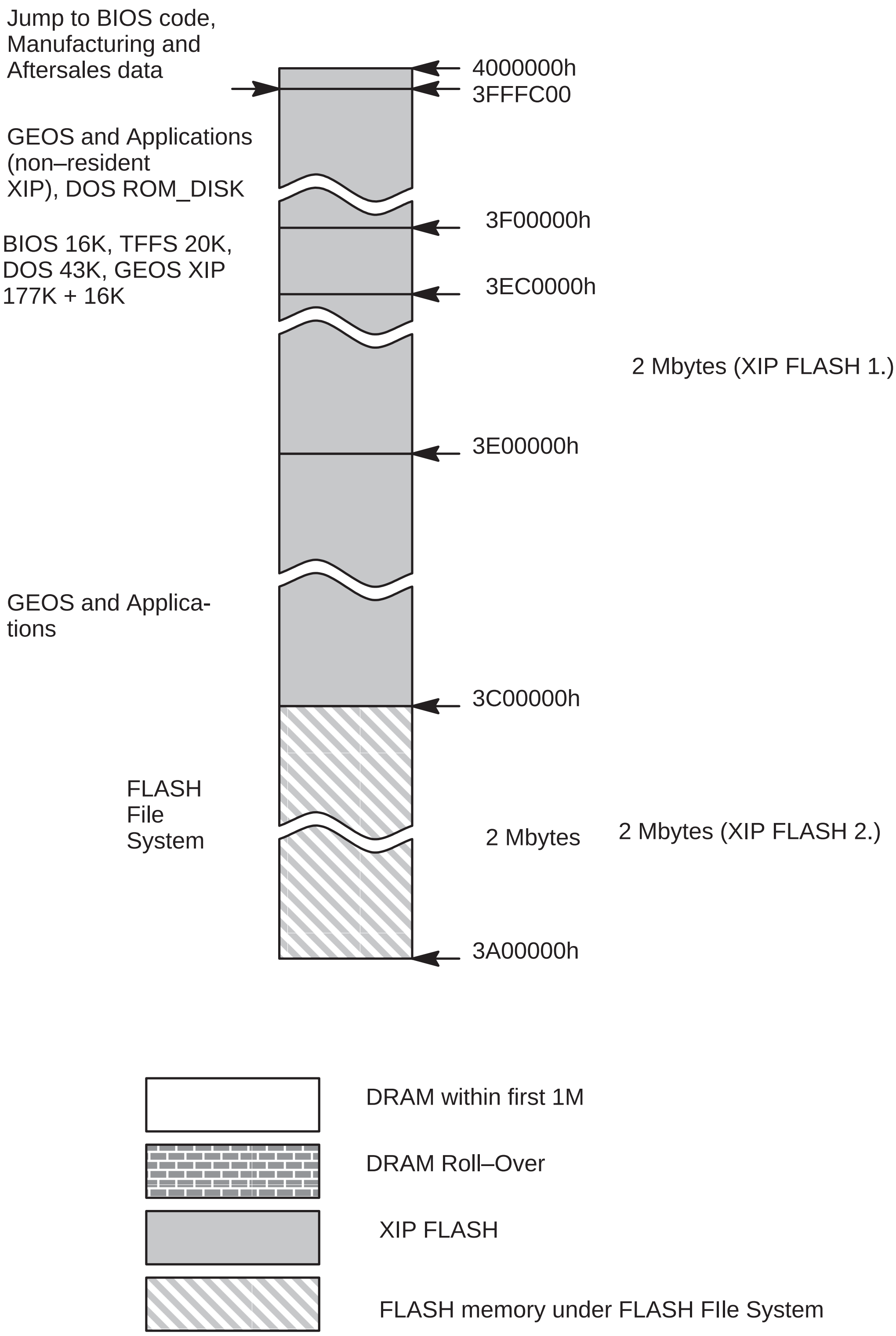

Figure 8. PROCU memory map part 3

– Chip selects

E3G CPU has four programmable chip selects. Size of the memory block can be defined with 2K resolution. Start address can be changed in 2K boundaries. These chip selects have independent programmable wait states (0–64).

Table 19. FLASH Chip Select Generation

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	CHIP SELECT	NOTES
1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	UCS XIP FLASH 1.	
0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	UCS XIP FLASH 1.	Double mapping
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	CS0 XIP FLASH 2.	
1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	CS1 RFD FLASH 1.	

DRAM controller enables shadowing in the area of 640KB – 1MB in 16–Kbyte granularity. Each block of memory can be configured as being disabled, read–only, write–only, or read/write. Unused memory in the area of 640KB – 1MB can be rolled over in 64–Kbyte granularity. Roll–over base is selectable in 512–Kbyte granularity.

– FLASH programming

PDA module FLASH memories can be programmed in two ways. During the manufacturing JTAG interface of the E3G CPU is used to download FLASH image to FLASH devices. For aftersales and R&D purposes BIOS is equipped with FLASH download capability via RS232. JTAG method is needed at aftersales as a backup.

During the manufacturing it is not possible to use any download method that needs CPU involvement because there is no any program code for execution on the device. JTAG interface was selected for this purpose because it exists on the E3G CPU and it is a standard. In principle JTAG interface is able to set CPU signals (address, data, etc.) to requested state. By changing signal values in reasonable manner FLASH writing is possible. Special hardware is needed for JTAG FLASH download during manufacturing as well as for aftersales purposes. JTAG FLASH download system is integrated to PTS and maintenance software.

RS232 FLASH load can be done with standard PC with a serial port and FLASH loading software. Upload is also possible with this software. On the PDA module RS232 FLASH download software is part of the BIOS. RS232 FLASH download commands are integrated to maintenance software.

FLASH programming voltage is generated on PDAPWRU. FLASH memory content validity can be checked by calculating error check code and comparing it to precalculated one.

– PROCU – PDAPWRU

PDAPWRU generates 3.3V VSYS for overall system usage and 5V for FLASH programming. FLASH programming voltage can be switched off with 5VPDX signal when it is not needed. Switchmode powersupplies are used for VSYS and LCD Vee. LCD display contrast control (bias) is generated by PWM unit in E3G CPU. This signal controls LCD Vee power supply on PDAPWRU. LCD bias and LCD logic voltages can be switched on and off by PROCU with LCDVEE and LCDVCC signals. PDAPWRU generates power good (PWRGOOD) signal for PROCU reset purpose. VBACK is always available for real time clock.

– PROCU – LCDM

640 x 200 LCD screen (8 actual grey scales) on LCDM is controlled by PROCU. Soft keys and scroll keys on LCDM module are connected to the keyboard controller on PROCU.

– PROCU – SIRU

IrDA transceiver and RS232 buffer are located to SIRU. Same RXD and TXD lines are used for both devices. When the device is not used the transmit line must be in high impedance state. Only one device is allowed to be enabled at a time. RS buffer have two control signals. RSENX to enable transmit line and RSSHDX to enable charge pump. IrDA tranceiver is enabled with IRSHD signal. External RS232 signals meet EIA/TIA–232 specification.

– PROCU – EMIU

EMI Unit is passive unit to reduce EMI noise on the lines that are located out of the shielding.

I/O usage on E3G CPU

The E3G CPU have configurable I/O pins that are used like described on Table 21.

Table 20. I/O usage on E3G CPU

Signal name	E3G CPU pin	Polarity	Reset value
PWRGOOD	RESET#	H = Power good	– (In)
5VPDX	PMI2 / P45	L = Shut down	L
TESTMODEX (Input)	DTR0# / P02	L = Test mode	– (In)
IRSHD	RI1# / P13	H = Shut down	H
RSSHDX	DSR0# / P00	L = Shut down	H
RSENX	CTS0# / P04	L = Enabled	H
XPWRON	PMI3 / P44	H (pulse) => CMT ON	L
FLASHPD1X	SUSPEND#	L = Shut down	H
FLASHPD2X	RI0# / P03	L = Shut down	H
FLASHWP1X	DCD0# / P01	L = Protected	H
FLASHWP2X	CTS1# / P15	L = Protected	H
LCDVCCON	LCDVCCON	H = Vcc ON	L
LCDVEEON	LCDVEEON	H= Vee ON	L
DISPON	DISPON	H = Display ON	L
”LID”	PMI0	H = Lid open	– (In)
VL1	PMI1	H = CMT ON	– (In)

I/O map

All chipselects are generated in the E3G.

Table 21. I/O Map

Device	Address	Note
PIC0	0020 – 0021	Standard PC compatible
PIC0	F022h	Edge / Level control E3G Specific
Timers 0 – 2	0040h – 0043h	Standard PC compatible
Port B	0061h	Standard PC compatible
RTC Offset	0070h	Standard PC compatible
RTC Data	0071h	Standard PC compatible
Port 92	0092h	Standard PC compatible
PIC1	00A0h – 00A1h	Standard PC compatible
PIC1	F0A2h	Edge / Level control E3G Specific
COM2	02F8h – 02FF	Standard PC compatible
COM1	03F8h – 03FF	Standard PC compatible
DRAM controller	F300h – F323h	E3G Specific
IRDA Select Register	F3F8h – F3F9h	E3G Specific

Table 21. I/O Map (continued)

Device	Address	Note
Chip Select Unit	F400h – F463h	E3G Specific
E3G Clock Unit	F800h, F87Bh	E3G Specific
E3G Bus Control Unit	F810h – F813h	E3G Specific
E3G Chip Configuration Registers	F820h – F825h	E3G Specific
E3G I/O Ports Unit	F860h – F87Bh	E3G Specific
E3G LCD Controller	F900h – F925h	E3G Specific
E3G PWM Unit	FC00h – FC01h	E3G Specific
E3G EMS Registers	FC10h – FC1Bh	E3G Specific
E3G Key Scan Unit	FC30h – FC39h	E3G Specific
E3G Power Management	FCA0h – FCB3h	E3G Specific

Interrupt map

The interrupt control unit inside the E3G contains two 8259A modules, connected in a cascade mode.

Table 22. Interrupt map

PC INT#	IRQx	Vector (hex)	Name	PC use
2	NMI	8	PMU INT	Parity Error / IO Check
8	IRQ0	20	Timer 0	same
9	IRQ1	24	Key Scan logic	8042 Keyboard
A	IRQ2	28	cascade vector	same
B	IRQ3	2C	COM2 (RBUS)	same
C	IRQ4	30	COM1 (RS232)	same
70	IRQ8	1C0	RTC	same
72	IRQ10	1C8	Timer 1 (Not used but available)	ISA

Main components

– E3G CPU

80386 based CPU. Static design. Using external clock source maximum clock rate 33MHz. With internal PLL's 23.96MHz. All needed peripherals are integrated to the same chip. Peripherals are as follows:

- Two cascaded Interrupt Controllers (8259A), DOS compatible
- Three programmable Timer/Counters, 8254 standard
- DRAM bus controller, no external buffers or multiplexers needed
- Chip select unit
- Real time clock (RTC)
- Two 16550 UART's with 16–byte FIFO's
- IrDA signal conditioning and RS232/IrDA select
- LCD controller (640 x200 8 actual grey scales)
- Pulse Width Modulator Unit
- 8 x 10 keyboard scan unit
- System power management unit
- Expanded Memory Specification (EMS) Unit
- 32 KHz Oscillator with Phase Locked Loop circuits to generate all needed frequencies
- JTAG (IEEE 1149.1) Boundary scan testing capability

E3G CPU is described in details in E3G EXTERNAL ARCHITECTURE SPECIFICATION, Intel Corporation 5000 West Chandler Blvd. Chandler, AZ 85226

– 1M*16bit FLASH memory 75 ns

- Intel 28F016SV 065
- 75 ns maximum read access time
- SMART voltage device with 5 Volt programming
- Used to store all program code
- 1 Million Erase Cycles Per Block
- Deep power down mode

- 1M*16bit FLASH memory 120 ns
    - Intel 28F016SV 070
    - 120 ns maximum read access time
    - SMART voltage device with 5 Volt programming
    - Used to store application data under FLASH File System
    - 1 Million Erase Cycles Per Block
    - Deep power down mode

- 1M*16bit DRAM memory
    - 70 ns maximum access time
    - Fast Page Mode
    - CAS before RAS refresh
    - CAS before RAS self refresh
    - Refresh block size 1K

- QWERTY–keypad
    - Hard top rubber keymat with carbon contacts
    - 56 QWERTY keys and 9 function keys
    - Key ON resistance < 1kohm
    - VT100 emulation compatibility keys included

PDAPWRU

Technical Description

The power block creates supply voltages for the PROCU and LCDM, generates reset signal for CPU and contains LCD contrast control and enable circuits. Input filter is required to reduce input noise of switching regulators. Back–up battery keeps RTC alive when main battery is not connected. System voltage is present allways until battery voltage drops below 5.0V.

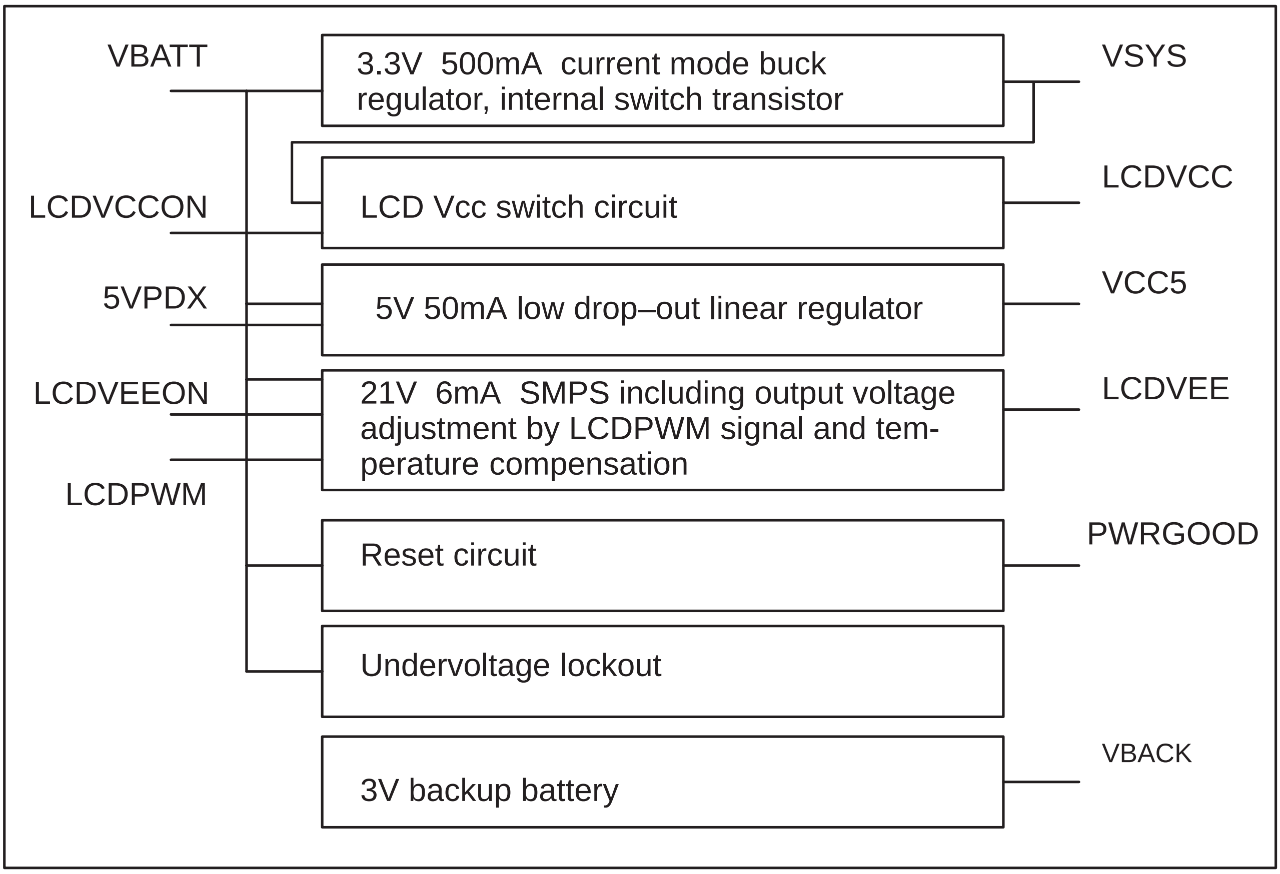

Figure 9. PDAPWRU block diagram

Table 23. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
LCDVCCON	LCD Vcc on/off	PROCU
LCDVEEON	LCD Vee on/off	PROCU
LCDPWM	PWM signal for LCD voltage control	PROCU
5VPDX	5V regulator powerdown	PROCU
VB	Battery voltage	B2B / VB

Note 1. B2B = Board to board connector between PDA and CMT modules

Table 24. External Signals and Connections, Outputs

Signal Name	Signal description	To (1)
VSYS	System voltage 3.3V	PROCU, SIRU
VCC5	5V for FLASH and RBUS	PROCU
PWRGOOD	Reset signal for CPU	PROCU
VBACK	Backup battery voltage to RTC	PROCU
LCDVCC	LCD Vcc to LCDM	LCMCON / LCDVCC
LCDVEE	LCD Vee to LCDM	LCMCON / LCDVEE

Note 1. LCMCON = LCD module connector on PDA module

Table 25. Electrical characteristics

Parameter	Mini-mum	Typi-cal	Max-mum	Units	Notes/conditions
Input voltage range of VB	5.0		11.0V	V	maximum no–harm voltage of VB line
Battery voltage VB	5.0	7.2	8.8	V	max voltage is during charge pulses with cycled battery
VSYS shut-down	4.9	5.0	5.1	V	VB for shutdown operation
	5.9	6.0	6.1	V	VB for cancel of shutdown
VSYS	3.135	3.3	3.465	V	tolerance over temperature and load range
		100	450	mA	output current, regulator I_{max}=500mA
		85		%	efficiency at I_{out}=200mA VB=6.0V
		82		%	efficiency at I_{out}=200mA VB=8.0V
		68		%	efficiency at I_{out}=10mA VB=8.2V
		86		%	efficiency at I_{out}=10mA VB=5.5V
	25	40	100	mV	output voltage ripple
		1.4	3	mA	supply current, no load connected
	159	200	212.5	kHz	oscillator frequency
LCDVEE	18	22	25	V	depending on temperature, typical value at room temperature
	1.3	2	3.5	mA	output current, regulator I_{max}=6mA
		75		%	efficiency at I_{out}=2mA VB=7.2V
			250	mV	output voltage ripple
		0.78		mA	supply current, no load
		330		kHz	operation frequency

Table 25. Electrical characteristics (continued)

Parameter	Mini-mum	Typi-cal	Max-mum	Units	Notes/conditions
VCC5	4.825	5.0	5.175	V	tolerance over temperature and load range
		120	225	mV	dropout voltage at I=50mA
		30		mA	regulator I_{max}=50mA peak current 100mA
		0.4	1.2	mA	ground pin current (supply current)
PWRGOOD	3.04	3.08	3.11	V	reset threshold at room temperature
	140	240	560	ms	power–on reset pulse width
		30		ppm/C	reset threshold temperature coefficient
VBACK	2.5	3.0	3.2	V	
		7		µA	nominal load when used
		130		mAh	capacity, charging not possible
Operating temperature range	–25		+85	°C	some circuits tolerate wider temperature range

Functional Description

VSYS regulator

System voltage regulator is current–mode pulse width modulation (PWM) dc–dc step–down converter. It has internal switch transistor and current sense resistor for current–mode control. Oscillator makes the switch transistor to turn on at fixed frequency. Switch transistor on time is determined by load taken at output. Current mode feedback makes transient response fast and provides cycle by cycle current limiting. This means that outer loop determines threshold voltage for current sense amplifier to reach to turn switch transistor off. Inner current feedback loop makes response to load current changes fast.

Outer feedback loop takes output voltage information and compares it to reference and drives the error towards zero in order to keep regulation. This kind of control keeps good regulation at output in rapidly changing load conditions. Tradeoff is high operation current in very light loads because oscillator is running all the time.

VSYS regulator operates at discontinuous conduction mode (DCM) at light loads. This means that current through inductor decreases to zero before new switch transistor turn–on pulse comes and current through inductor starts to increase. At heavy loads inductor current does not go to zero and operation is in continuous conduction mode (CCM).

The controller has internal 1.23V bandgap reference and soft start circuitry for power–up. Overcurrent comparator disconnects the controller in short circuit conditions. After this soft start cycle is made in power–up. Output ripple voltage is determined by output capacitor ESR value which is minimized to reduce EMI. Shutdown mode is used when battery voltage decreases down to 5V to prevent battery from overdischarge. In shutdown all circuits are in lowest power state.

LCDVEE regulator

LCD bias voltage is made by step–up dc–dc controller. Control scheme is current limited pulse frequency modulation (PFM). External switch transistor and current sense resistor are required. Maximum inductor current goes through current sense resistor. Because required regulator output current is small (3mA), resistor value is selected so that current through inductor is low to reduce EMI. Also switch transistor ON–resistance need not be lowest possible. Pulse frequency control is made without oscillator, maximum on–time and minimum off–time are used in pulse control. When output voltage is out of regulation the switch turns on and it stays on until maximum on–time turns it off or inductor current reaches its maximum value set by current sense resistor. When the switch turns off, minimum off–time is waited.

After this the switch stays off until output voltage drops out of regulation. This control results current pulses which are delivered on load demand and ’skipped’ when in regulation, ’pulse skipping’ regulation. Benefits are very low supply current at light loads because of no oscillator and high energy conversion efficiency. Because pulses come at unspecified time intervals switching noise is in broad frequency range. However maximum inductor current is set to lowest practical value and output capacitor ESR is selected for low value to reduce EMI.

Output voltage is adjusted by LCDPWM signal from PROCU. This pulse width modulated signal is first converted to analog dc voltage by RC–filter. This signal is fed to regulator feedback pin through a resistor which determines the scale at which the LCD display bias voltage can be adjusted. Temperature compensation for bias voltage is made by resistor divider connected to regulator feedback pin. Bias voltage is controlled by two NTC resistors so that optimum LCD contrast bias voltage is followed accurately by the regulator in temperature range between –20°C and +65°C. Because feedback pin comparator voltage is 1.5V and regulator output voltage is over 20V high accuracy feedback resistors are needed for fairly accurate output voltage.

Shutdown is controlled by PROCU. Because this is boost regulator there is current path from input to output which must be cut separately in shutdown. Control switch is placed between regulator output and load.

VCC5 regulator

5V output is used only for data writing to FLASH memory and RBUS signals. Regulator is taken out of shutdown when it is needed. This simple linear regulator has pnp control transistor and overcurrent/overtemperature protection circuitry. Maximum current is 50mA. Peak current is 100mA. At higher loads case heats up and regulator is shut off for very short time and restarted to check if high load remains. If so thermal cycling results. Typical turn–on time for the regulator is 50µs. Only small output capacitor is needed as external component. However, its ESR value must be within certain limits depending on capacitance and load current in order to get stable regulator output.

Reset circuit

Purpose of the reset circuit is to generate proper reset to the CPU and also disable CPU operation when Vsys is below CPU Vcc range. When the battery is plugged in reset circuit generates proper reset pulse when Vsys is risen up to CPU Vcc range. Threshold difference between ”power good” and ”power not good” is about 0.02V.

Undervoltage lockout (UVLO)

Battery voltage is compared to accurate reference diode to detect too low battery voltage. Below this HW limit comparator shuts down VSYS regulator to prevent battery from overdischarge. There is higher SW limit for PDA but VSYS regulator current drains the battery when left unused for long period. After UVLO there is only reference diode and two comparators taking current from battery. UVLO has hysteresis and is cancelled when battery voltage is risen to 6.0V. Only way to do this is by charging or plugging in fresh battery. Hysteresis is made to avoid unsuccessful power–ups. When lockout voltage level is reached battery voltage rises because load is removed.

Input filter

LC–lowpass filter is used between battery and regulators. EMI is not big problem in regulator outputs but EMI conducted from switchmode regulator inputs to battery line needs filtering. Also attenuation of EMI from CMT devices in battery line to PDA regulators is welcomed. Good ground planes and placement of PDA power block to metal cavity and low output ripple voltages keep radiated EMI at low level.

Backup battery

Real time clock is kept running by backup battery only when main battery is not connected. At nominal RTC load 130mAh capacity of backup battery gives over two years of RTC operation when main battery is not connected. Backup battery is not chargeable.

Main components

- 3.3V current mode PWM controller IC
  - MAX763AESA from Maxim
- 5V linear regulator
  - LP29801M5–5.0 from National Semiconductor
- 21V switch mode PFM controller IC
  - MAX772ESA from Maxim
- PWRGOOD reset circuit
  - MAX809T from Maxim
- 3.0V primary back–up battery, 130mAh
  - CR2320 with custom made pins from Matsushita

SIRU

Introduction

IrDA transceiver and RS232 buffer are located to this module. Infrared interface conforms to the Infrared Data Association Serial Interface (SIR) Physical Layer LInk Specification.

SIRU functions:
– external interface signalling (IrDA and RS232)

Technical Description

Table 26. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
VSYS	System voltage 3.3V	PDAPWRU
TXD	External serial data from 9000	SC / SYSTXD
RSTXD	Serial data from PROCU module	PROCU
RSENX	RS buffer enable	PROCU
RSSHDX	RS buffer shutdown	PROCU
IRSHD	IR tranceiver shutdown	PROCU

Note 1. SC = System Connector

Table 27. External Signals and Connections, Outputs

Signal Name	Signal description	To (1)
RXD	External serial data to 9000	SC / SYSRXD
RSRXD	Serial data to PDA module	PROCU

Note 1. SC = System Connector

Main components

- IR tranceiver
  - Temic IrDA SIR integrated transceiver TFDS3000
  - Shutdown pin
- RS 232 buffer
  - MAX3222CAP transceiver from Maxim
  - Two transmitters, two receivers
  - Generates EIA/TIA–232 compatible signal levels

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Chapter 7

Service Software

CONTENTS – Service Software

List of Figures

Introduction

The Nokia 9000 service software is a dual purpose package designed to test all CMT and PDA functions by means of menu driven user interfaces; it is also used to download new flash images. The software requires that a dongle, PKD–1 , be fitted to the PC parallel in order to enable software functionality. This chapter details both service and flash downloading functions in separate sections.

Required Servicing Equipment

– Computer: IBM PC/AT or compatible with at least one, unused serial port, COM1 or COM2 (see note below), one parallel port (LPT1), hard disk recommended. DOS Version 3.2 or later

– Display: Any 80–character text display

– Service software program, LSD–1 for 3.5” disk (product code: 0774057)

Note: *Two ports are preferable. A number of PC’s of an older generation use the Intel, National Semiconductor, or United Microelectronics IC 8250 as the serial port UART. This is a comparatively inefficient circuit for current purposes and does not necessarily support the M2BUS adapter at 9600 baud. The newer UART’s NS16450 and NS16550AF of National Semiconductor offer solutions for these problems.*

A list of service tools ,accessories and part numbers are given in Chapter 9 of this manual.

Note *:– Screen shots for both PCN and GSM units are, in general, universal. Where they differ an extra screenshot is shown.*

Testing Functions

Mechanical Connections

Caution: Make sure that you have switched off the PC and the printer before making connections ! Do not connect the PKD–1 key to the serial port. You may damage your PKD–1 !

Attach the protection key PKD–1 to parallel port one (25–pin female D–connector) of the PC. When connecting the PKD–1 to the parallel port be sure that you insert the PC end of the PKD–1 to the PC (male side). If you use a printer on parallel port one, place the PKD–1 between the PC and your printer cable. The PKD–1 should not effect devices working with it. If some errors occur (errors in printing are possible) please try printing without the PKD–1. If printing is OK without the PKD–1 please contact your dealer. We will offer you a new PKD–1 in exchange for your old one.

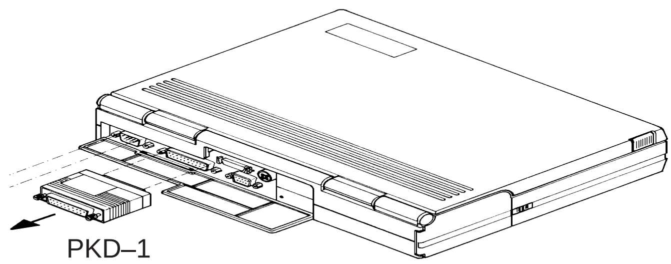


Figure 1. Dongle insertion

Connect up service tools as shown in Figure 2 overleaf. The dummy battery, BTD–1, contains the following leads:–

– The M2BUS lead (DAU–2/2T) – connect to COM1 (9–pin male D–connector); this is for testing the CMT module.

– Power leads – connect to suitable 7.2vdc power supply

DLR–1 should be connected to PAS–1 and to COM2 on the PC if available; this is for testing the PDA module. For PCs without COM2 leave disconnected until CMT testing is completed or use –p option to start the program (RAE_1) without CMT testing.

Note: *from version 1.3 –p option starts RAE_1 program directly for PDA usage*

When complete, switch on the communicator.

Note: *PAS–1 has a minimum mode switch. This switch should normally be left in the off state (switch pulled out). It is only used when a CMT flash download fails.*

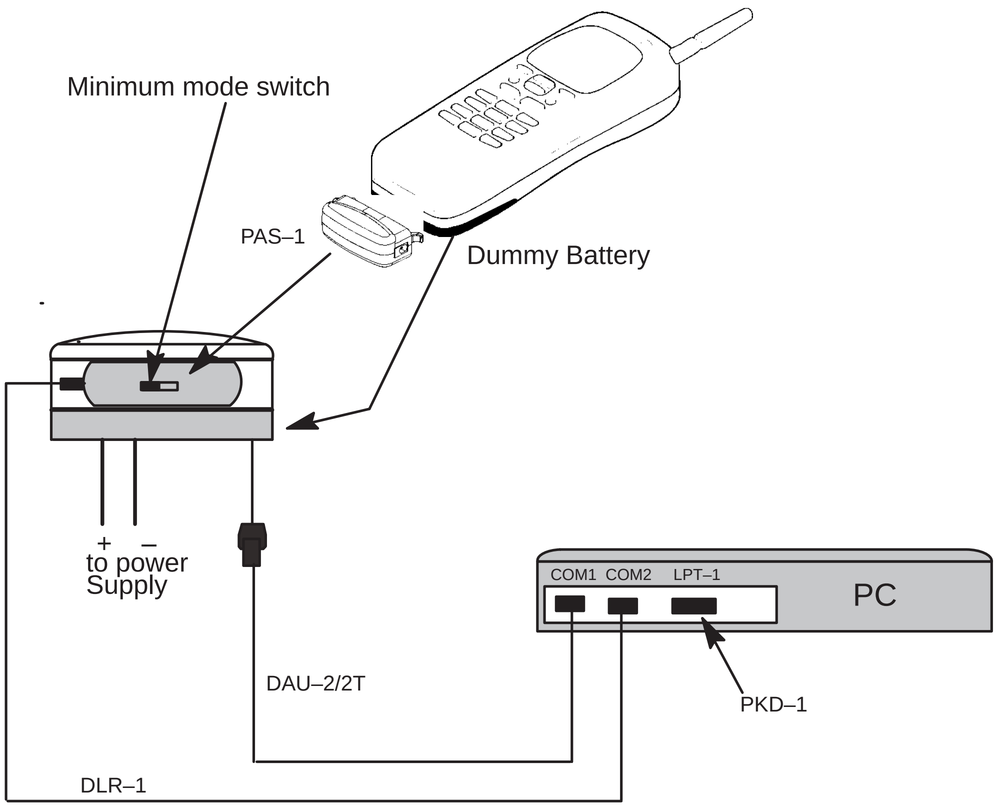


Figure 2. Servicing setup

Loading the Software

The program is delivered on a diskette and can also be installed on the hard disk, which is recommendable to obtain maximum data access rate.

Do not lose your original diskette. It will be needed when upgrading the program.

To start the program on diskette, proceed as follows:

1. Insert Service software diskette into drive A: of your PC
2. Log into drive A: *type A: press <Enter>*
3. To run software *type **rae_1** press <Enter>*

To start the program on hard disk (if installed), proceed as follows:

1. Log into drive C: *type C: and press <Enter>*
2. To run software *type **rae_1** and press <Enter>*

Complete Menu Structure

MAIN

1 Program setup
2 Initialize CMT
3 CMT Testing and Adjustment
4 CMT ME Memory Functions
5 CMT Power–up Self–tests
6 CMT SW and HW Versions
7 Phone Mode (Local/Normal)..:Local
8 PDA Functions
9 Faultlog
Q Quit

PC Setup
1 Load New Setup
2 Save Current Setup

CMT Testing and Adjustments
1 RF Controls
2 Adjustments
3 Call Simulation
4 Internal Audio Loop
5 External Audio Loop
6 Logic Controls
7 Run MCU Selftests
8 Set MCU Start–Up Self–tests

CMT ME Memory Functions
1 User Settings and Values
2 Product Profile Settings
3 Write HW Version
4 IMEI Edit
5 IMEI Transfer
6 Set UI Factory Values
7 Set Factory Values

CMT Power–up Selftests
MCU Internal Test.........................:OK
MCU RAM BUS Test.....................:OK
MCU IMEI Test..............................:OK
MCU ROM BUS Test:....................:OK
MCU ROM DATA Test...................OK
MCU ASIC BUS Test.....................:OK
MCU ASIC Timer & IRQX Test.......:OK
MCU ASIC Timer & NMI Test.........:OK
MCU Audio Codec Test..................:OK
MCU DSP Code Download...........: OK
MCU EEPROM Checksum Test: OK
MCU SIM LOCK ChecksumTests..: OK

CMT SW and HW Versions
MCU Internal SW Version.: 2.16 18–09–95 D8 (c) NMP.
MCU External SW Version: 2.61 18–03–96 GE8 (c) NMP.
DSP Internal SW Version..: ROM7 (MD)
DSP External SW Version.: G7.21CR
ASIC Version.....................: G–3
HW Version.......................: 0001
Manufacture month............: 0396

PDA Functions
1 Initialisation
2 Test Peripherals
3 Flash Utilities
4 DRAM Utilities
5 I/O Space Functions
6 Product information

CMT Menu Structure –Testing and Adjustment

Testing and Adjustments
1 RF Controls
2 Adjustments
3 Call Simulation
4 Internal Audio Loop
5 External Audio Loop
6 Logic Controls
7 Run MCU Selftests
8 Set MCU Start–up Self–tests

RF Controls
1 Actie Unit (TX/RX)............................: RX
2 TX Power Level................................: 15
3 Operation Mode (Burst/Continuous).: Burst
4 TX Data Type (0/1/RND).............:..... 1
5 Continuous Mode Channel...............: 60
6 Channel...: 60
7 Monitoring Channel...........................: 1
8 AGC...: 81
8 AFC...: –54

Adjustments
1 Continuous Mode Channel...........: 60
2 TX Power Tuning
3 TX I/Q Tuning
4 RSSI Calibration
5 AFC Diagram
6 Noise Sensitivity
7 Charge Voltage Adjustment
8 Battery Voltage Adjustment

Call Simulation
1 TX Power Level........: 10
2 Channel....................: 60
3 Monitoring Channel 1: 1
4 Monitoring Channel 2: 1
5 Monitoring Channel 3: 1
6 Monitoring Channel 4: 1
7 Monitoring Channel 5: 1
8 Monitoring Channel 6: 1

Internal Audio Loop
1 Input (Int/Ext/Phf)......: Int
2 Output (Int/Ext/Phf)...: Int
3 Loop (On/Off).....: Off

External Audio Loop
1 Interface (HS/HF/PHF)....: HS
2 Make a Measurement
FREQUENCY /Hz 300 1000 3000
RECEIVED LEVEL

Logic Controls
1 Read A/D Converters
2 LCD test display (1/2)...............: 2

Set MCU Start–up Self–tests
1 ASIC BUS tests.............. (On/Off).......Off
2 ASIC Timer & IRQX Test...(On/Off).....:Off
3 ASIC Timer & NMI Test......(On/Off):... Off
4 Audio Codec Test...............(On/Off)...: Off

CMT Menu Structure – ME Short Code Memory

CMT ME Memory Functions

1 User Settings and Values
2 Product Profile Settings
3 Write HW Version
4 IMEI Edit
5 IMEI Transfer
6 Set UI Factory Values
7 Set Factory Values

User Setting and Values
1 Lock ID. 35317
2 Master Code 5535021967
3 Wake up Message
4 No Service Power Save . . No

Product Profile Settings
1 CMT language (English /German /French) : English
2 Keyboard layout (Normal /AT&T/ /ITU–T) . . : Normal
3 A5/2 Algorithm . . . . (On /Off) . . . . : Off
4 SS Screen indicator . . . . . (1/2) . . . . : phase 1

Using Menus

You can select a function from a menu in two different ways. The first way is to press the key on the PC keyboard corresponding to the first character of the line. The other way is to move the cursor from line to line using arrow keys and make the selection with the <Enter> key.

When you have made your selection the new menu or window will appear. Every menu and window carries its name on the topmost line, this is the same as the selection in the previous menu or window. When the new menu is activated the old one will disappear.

When a window is activated the selectable keys are seen in the window. Windows may have a scrolling or a constant display.

The <Esc> key quits the previous menu and returns the previous screen, it has no effect if used with the main menu. When editing data the <Esc> key can be used as an interrupt key and the <Enter> used as an exit key.

Help Functions

The help key <F1> can be used anytime when a menu is on the display. The help key is context–sensitive and gives information according to which function is highlighted. The <Esc> key closes the help window..

Text Editing Windows

When you have made a selection which needs some additional information, the basic text editing window is activated.

The text editing window may have one or more editing lines. The length of the line varies depending on the function. When the window is activated the text which was previously in that window (default text) reappears on the screen.

The following key selections are possible:

Key	Function
<Enter>	Selects the text in the window; the editing window is turned off. The selected text will be the default text of the selection.
<Esc>	Interrupts editing; the previous menu is shown and the default text won’t be updated.
<Ins>	Toggles the editing mode between insert and overstrike modes. The last line of the screen tells the current editing mode. When editing ends, the editing mode is retained and the same mode is used again when editing text.
<←> < >	Arrow keys (right shift and left shift) move the cursor. The cursor moves as if the lines were positioned one after another. For instance right shift causes the cursor to move from the last column of the first line to the first column of the second line. If the right shift is used and the cursor is at the last position of the last line, the cursor is not moved. Similarly, the cursor does not move with the left shift key when it is at the first position of the first line.
<Home>	Moves the cursor to the start of the text.
<End>	Moves the cursor to the end of the text.
<BS>	The backspace key has two different meanings depending on the editing mode; •When the overstrike mode is activated the <Backspace> key moves the cursor back and changes the character under the cursor into a space. If the cursor is at the first position of the first line nothing happens.

• When the insert mode is activated the <Back space> key moves the cursor back and deletes the character under the cursor so that all characters after the deleted character are moved one position back. If the cursor is at the first position of the first line nothing happens.

<Del> Has also two different meanings depending on the editing mode;

• When the overstrike mode is activated the <Del> key changes the character under the cursor into a space and moves the cursor forward. If the cursor is at the last editing position of the last line nothing happens.

• When the insert mode is activated the <Del> key removes the character under the cursor so that all characters after the removed character are moved one position back. If the cursor is at the last editing position of the last line nothing happens.

<F1> Function key number 1 activates the help window.

<F4> Clears text in the editing window.

CMT Menu Commands

When you start the program, the phone will initialise if correctly connected. It not an error message will appear. Once initialised, the main menu can be seen on the screen; there are nine main functions;

The phone defaults to ‘Normal’ mode and functions 3 and 4 are inaccessible in this mode. Select function 7and press enter to change to ‘Local’ mode for all test purposes.

The number identifier of each title in this chapter refers to a main function, menu and sub–menu items. E.g.

– 3 Test and Adjustment – main function
– 1 Rf Control –menu
– 2 Tx Power level –sub menu

1 – PC Setup

When **Save Current Setup** is selected the program asks for a setup file name. The saved information will include all parameters shown below:

- Command line parameter value for COM–port selection

– RF Controls menu

- All selections

– Call Simulation

- All selections which are not the same as in the RF Controls menu

– Tuning parameters (PC default values; no effect on EEPROM values)

- TX power coefficients
- Power connection diagram

– Run MCU Self–tests

- All selections

The following selections are <u>not saved</u> to the setup file:

– Values which are asked from MS

- AFC value

– Main Menu

- Phone Mode (Start value = Normal)

– PC Setup menu

- Default name for setup file
  (Start value = RAE_1.CON)

– Internal audio loop:

- input (Start value = Int)
- output (Start value = Int)
- loop (Start value = Off)
  – External audio loop:

- interface (Start value = HS)
  – Logic controls

- LCD Test Display (Start value = 1)

Load New Setup – generates the same kind of message as the save function and asks for a setup file name. When the name is keyed in and entered <Enter>, the file is loaded and all previously selections and parameters are replaced with the values taken from the file. This has same effect as command line parameter –f.

Both **save file** and **load file** functions have default names which are generally the previously used name. For instance, if setup was saved to file CONF.CON and the **load file** function is activated, the default value becomes CONF.CON. Press the ENTER key to accept these files parameters or press the BACKSPACE key to clear entry and key in another filename and then press ENTER. The<Esc> key returns to the previous menu. Invalid DOS filenames will give an error message.

If phone mode had Local value before setup file loading, the mode is changed to Normal in the phone by special Normal mode message and all functions caused by the change are done. If mode was Normal before new setup, all needed setup file settings are sent to MS as in the previous case, but phone mode change command is not sent to MS. Note next exception: If phone mode is Normal and interface is M2BUS and communication port is different in the setup file than the value before file loading, then also Normal phone mode message has to be sent to MS.

Every time when phone mode change message from Local to Normal is received by MS it makes reset to the whole MS.

2 – Initialize Phone

With this function you can initialize the phone to accept M2BUS commands from the PC. This function should be used right after the phone is connected to PC and powered up. This function also asks for the PIN code if the phone’s PIN asking is activated.

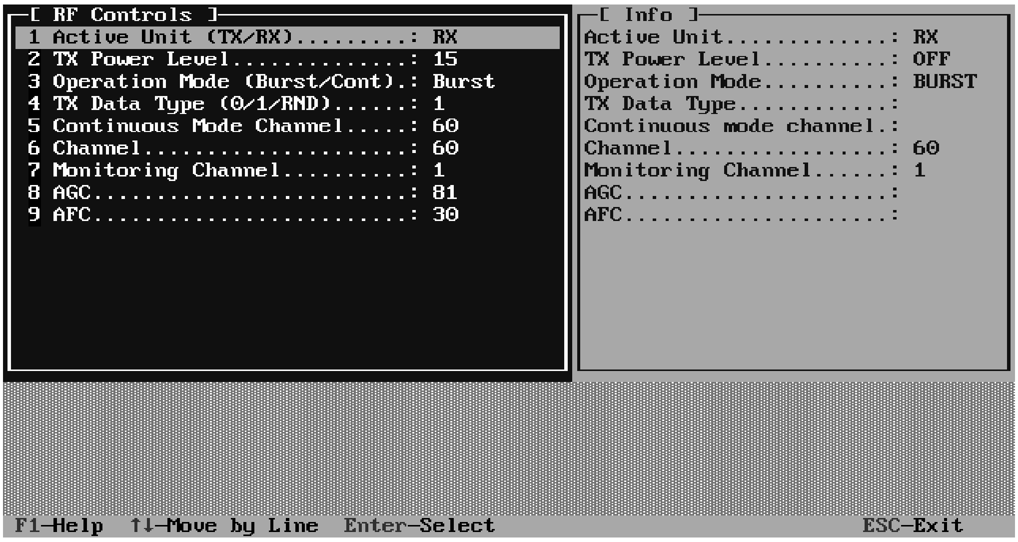
The initialization function performs the following subfunctions:

– MBUS registration
– Test mode message sent to the phone
– Phone mode set to GSM
– AFC value removed from info window

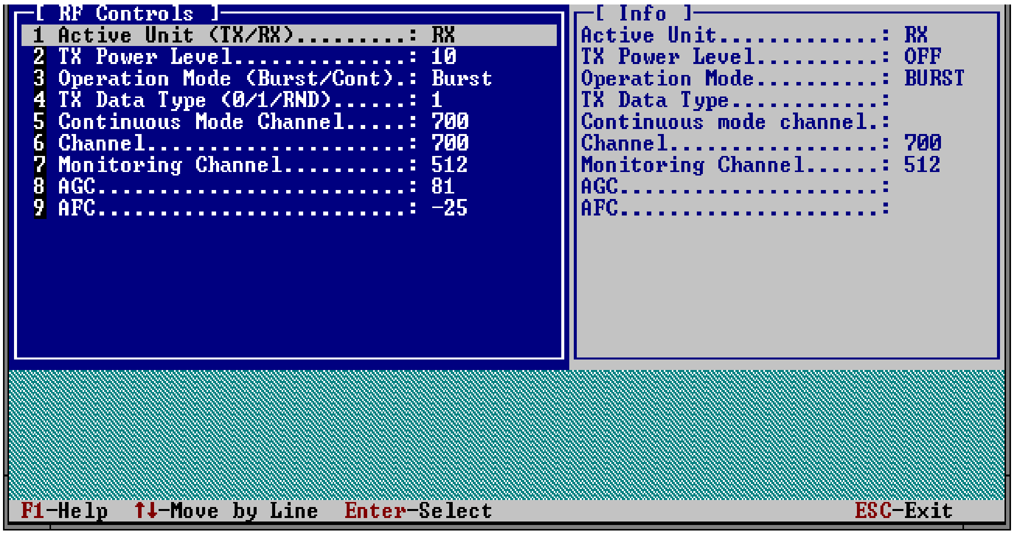
3 – Testing and Adjustments

When testing and adjustment menu is selected, the phone mode must be set to the ‘Local’ value. If the local mode is not set, an error message is shown.

3.1 – RF Controls



GSM Version



PCN Version

RF Control Information Window

When RF controls menu is activated, the information window is generated and updated when information is changed. This window closes when exiting the RF controls menu.

The next table shows the information window display on different situations:

Active Unit = TX	Operation mode = BURST	Operation mode = CONT.
TX Data Type: AGC Values: TX Power Level: Continuos Mode Chan- nel: Channel: Monitoring Channel:	Updated Removed Updated Removed Updated Updated	Not in use Not in use Not in use Not in use Not in use Not in use

Active Unit = RX	Operation mode = BURST	Operation mode = CONT.
TX Data Type: AGC Values: TX Power Level: Continuos Mode Chan- nel: Channel: Monitoring Channel:	Removed OFF OFF Removed Updated Updated	Removed Updated OFF Updated Removed Removed

Note: *Continuous mode with TX active unit is not possible*

3.1.1 – Active Unit

Either receiving or transmission tests can be selected. When TX is selected, Data transmission is activated :

● If operation mode is continuous,
– Continuous mode is changed to burst mode,
● If operation mode is burst,
– TX power is activated
– TX channel is activated
● Information window is updated

When RX is selected, Data transmission is deactivated

● TX power is deactivated
● if operation mode is continuous,
– AGC is controlled
– Continuous mode RX channel is activated
● If operation mode is burst,
– RX and monitoring channel are activated
● Information window is updated

3.1.2 – TX Power Level

With this function it is possible to change the transmission power. When the selection is made, the user can give the needed GSM power value (5...15) or select the test value, which is tuned with TX power tuning function. The test value selection is made by writing ”test” with small or capital letters.

3.1.3 – Operation Mode

When burst selection is used,

– synthesizer is controlled by using GSM/PCN receiving/transmission /measuring synthesizer control sequence
– synthesizer channel numbers are as given with Channel/Monitoring Channel selections
– if Active Unit is TX, data (selected with TX Data Type) is sent and the TX power is connected

When continuous selection is used,

– if Active Unit is TX, operation mode is changed to burst mode and functionality is same than when burst selection is used
– synthesizer is set to a constant frequency
– synthesizer channel number is as given with Continuous Mode Channel selection
– when Active Unit is RX, AGC is controlled

3.1.4 – TX Data Type

This function changes the transmission data type. Every time when selection is made, the next value in the list is shown (i.e. 0/1/Random). After random data, selection 0 is used.

3.1.5 – Continuous Mode Channel

Continuous mode may use any GSM/PCN channel numbers (GSM: 1...124 PCN: 512....885). The used frequency depends on the active unit. When active unit is RX, then RX frequency is used. If active unit is TX continuous mode channel is ignored.

3.1.6 – Channel

”Channel” selection numbers are used for both transmission and receiving.

3.1.7 – Channel; Monitoring Channel

”Monitoring channel” is selected separately for a neighboring monitoring channel. All GSM/PCN channel numbers (in GSM phone: 1...124 PCN: 512....885) are valid.

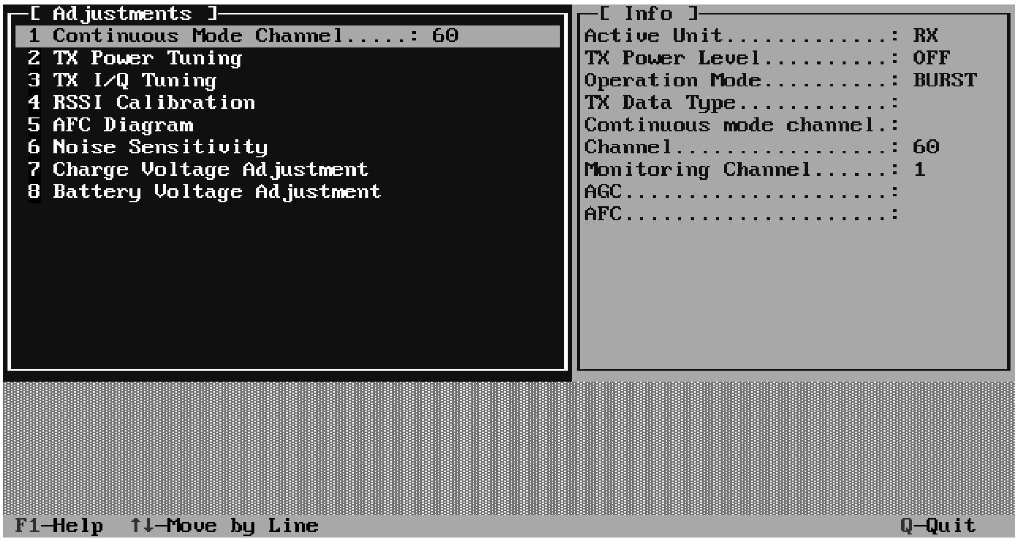
3.1.8 – AGC

The AGC can have values of 0...93 dB by 3 dB steps. If the number is not divisible evenly by 3 the number is rounded to the next bigger number divisible by 3. Only the number can be edited (not letters dB).

3.1.9 – AFC

Sets the AFC D/A converter value. This can have values from –1024 to 1023.

3.2 – Adjustments



All adjustments which have EEPROM saving selection have the next kind of behaving with F2 and ESC keys.

When adjustment function is activated and <F2> key is used the program will ask are the values saved to the EEPROM or not. If <Y> key is used, adjustment values are saved to the EEPROM. If <N> or <Esc> key is used the adjustment can be continued. If any other key is used nothing happens.

When <Esc> key is used during adjustment function, the program will ask are the values saved to the EEPROM or not. If <Y> key is used, adjustment values are saved to the EEPROM and exit from the function is done. If <N> key is used exit is done from the function and nothing is saved to the EEPROM. If <Esc> key is used the adjustment can be continued. If any other key is used nothing happens. When exit is made from the adjustment menu, the used adjustment values are used with the normal DSP control commands in the local mode (i.e power connection diagram and power levels).

3.2.1 – Continuous Mode Channel

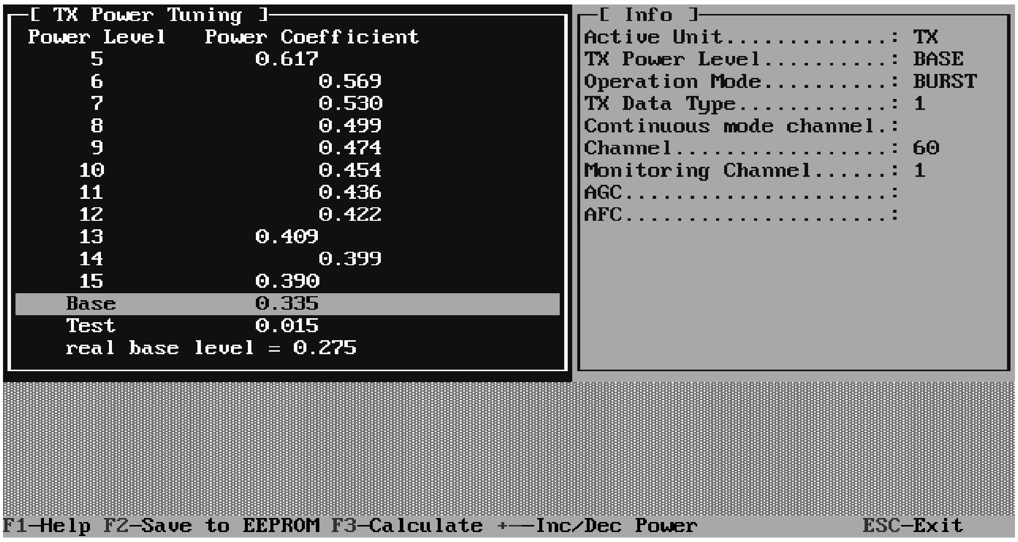
Continuous mode channel number can be selected from the Adjustments menu. The real frequency (transmission or receiving frequency area) depends on the Active Unit selection and the selected tuning function. Active Unit defects to the frequency when no selection is made from the Adjustments menu. Note that this is same selection as in the RF Controls menu.

3.2.2 – TX Power Tuning

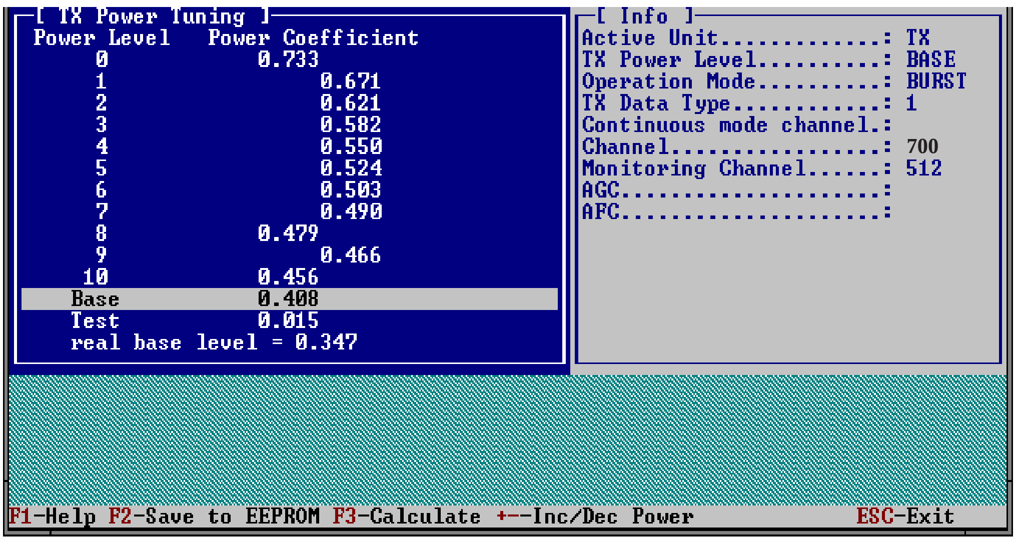
Once selected the display asks the following:

Note: Base Power level activated unless
command is interrupted by ESC
Do you want to load Values from EEPROM?
(Y/N) _

If <Y> is selected, tuning values from EEPROM are loaded. If <N> is selected, the values which the PC program normally uses when DSP is controlled are used. ESC returns to the previous menu. PC program values are tuning settings which are used for DSP control in the local mode.



GSM Version



PCN Version

There is one selection which is used for power coefficient calculation. Only three power coefficients (biggest, third smallest and smallest) are needed for tuning, the rest are calculated.

The calculation is activated with <F3> key. The power coefficients which are calculated from the tuned coefficients are displayed on the different columns than the others. All values can be tuned if needed.

The following automatic selections are made when this tuning function is activated:

– if transmission data is neither 0 nor 1 then continuous 1 data is selected
– Active Unit = TX
– the base power level is selected
– Operation mode = Burst
– Channel = 60

<+> and <–> keys will cause power changing by 0.25 dB steps (D/A converter control value ratio is 1.0292). When these keys are used the coefficient value is updated on the tuning window.

When save <F2> or exit <ESC> selection is used, the power value checking is made and if it is not successful, an error message is shown. The test checks if all power coefficient values are in the same numerical order as Power Levels in the table.

When TX Power Tuning is ended and if the power values are not acceptable, the error message is displayed and the user is asked to continue or break the tuning. These responses are in use:

Key	Response
N or Esc	The tuning is continued
Y	The tuning is ended without EEPROM writing and power coefficients are asked from EEPROM (the user is informed.)
other key	–

If the power tuning function is ended and EEPROM values are not received or an EEPROM fault is noticed, an error message is shown. Error message asks to initialize the phone and if initialization is performed successfully the program is restarted.

If this kind of error situation appears restart program, check connections and retune.

If the TX Power Tuning is ended and power coefficients are acceptable,

Key	Response
Y	The coefficients are written to EEPROM and tuning is ended
N	The tuning is ended without EEPROM writing but the tuned coefficient values are used when RF controls are used
Esc	The tuning is continued
other key	–

When all power co–efficients have values that don’t cause any error messages, exit can be selected. The latest tuning power is in use after exit.
When values are saved to EEPROM, GSM levels 0...5 are set to same value as level 5.

The next automatic selection is made when this tuning function is ended:

– Active Unit = RX

3.2.3 – TX I/Q Tuning

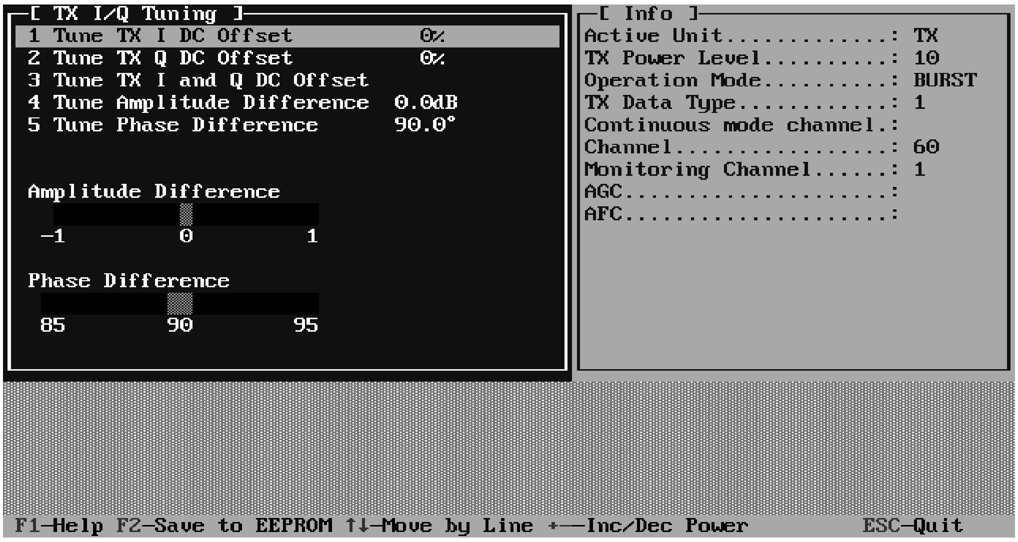
This function is used for tuning TX I and Q branch DC offset, amplitude difference and phase difference.

The function asks the same questions about values (from EEPROM or PC) as power tuning.

The following automatic selections are made when this function is activated:

– Active Unit = TX
– Operation Mode = Burst
– TX Power Level = 10 (GSM)
– If TX Data Type= RANDOM => TX Data Type= 1
– Channel = 60 (GSM)

The next menu is displayed after the answer.



When a selection is made, the menu will disappear from the display and the control will be on the tuning window.

The right top hand corner of the tuning window shows which tuning is activated. The user can tune the current value with the plus <+> and minus <–> keys.

Tune TX I DC Offset

The DC Offset is shown as a percentage of the maximum value. 0 % means that there is no DC. The value range is –100 %...100 %. The value is rounded to the nearest integer value.

Tune TX Q DC Offset

The operation of this function is the same as the previous one, except with this selection, the Q branch DC Offset is tuned.

Tune TX I and Q DC Offset

The operation of this function is the same as the previous one, except with this selection, both I and Q branch DC Offset is tuned. When plus <+> or minus <–> key is pressed, both values are changed to the same direction. If another value is in the limit value it does not change, but the other value will change.

Tune Amplitude Difference

When this selection is made the user can increase or decrease the amplitude difference within 0.1 dB steps. The current amplitude difference is shown on the tuning window with numbers and a bar figure.

Tune Phase Difference:

When this selection is made the user can increase or decrease the phase difference within 0.5 steps. The current phase difference is shown on the tuning window with numbers and bar figure.

After each value change the new values are sent to the phone.

The following is requested when TX I / Q tuning function is ended:

– Write values to EEPROM (y/n)

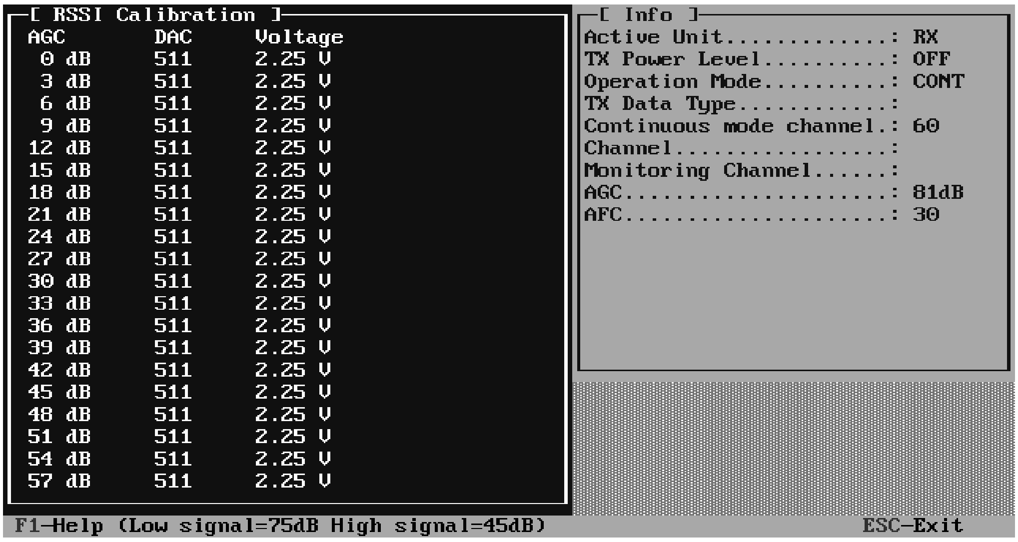
3.2.4 – RSSI Calibration

When function is activated the selected channel is checked. If none of the receiving channel numbers from 50 to 70 in GSM mode and 670 to 730 in PCN mode is selected then an error message is shown and the user is asked to change the channel to the valid receiving channel area.

The following automatic selections are made when this tuning function is activated:

– Active Unit = RX
– Operation Mode = Continuous

The next window will be seen when the tuning function is selected.



RSSI offset value and AGC compensation terms have 0.1 dB precision.

The RSSI offset value and AGC compensation terms are read again when the previous values are received and results are shown on the screen.

If no measurement result is received when <Esc> key is used, an information message is shown. The user can remove the information message with <Y>, <N> or <Esc> key. The measurement will be terminated by using the Y key.

The measurement will continue if <N> or <Esc> key is used.

When at least one measurement is done and <Esc> key is used, the user must answer to the values saving question. If <Esc> key is used, the measurement is continued.

Upon exiting, the next selections are set to the values which were selected before this adjustment.

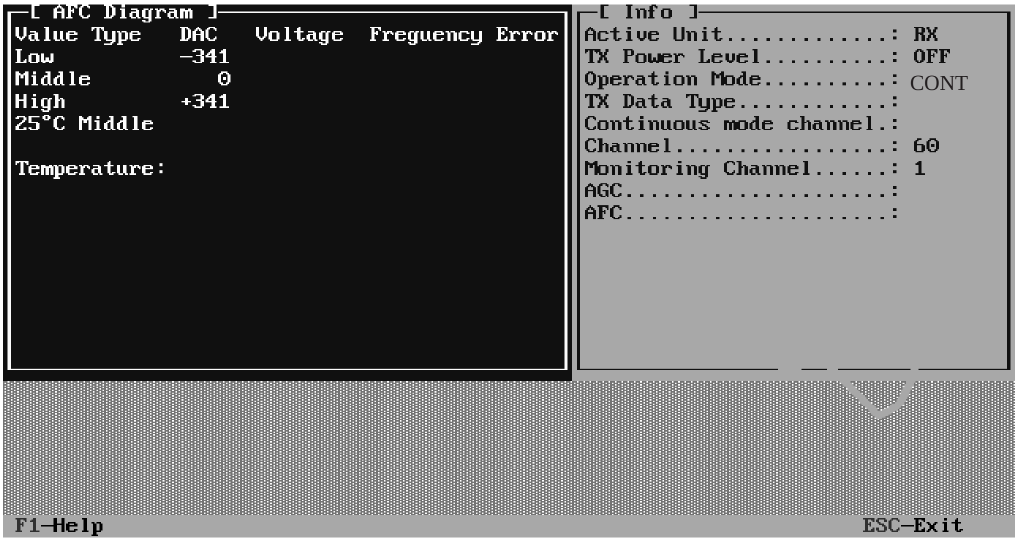
– Active Unit
– Operation Mode

3.2.5 – AFC Diagram

The following automatic selections are made when this tuning function is activated:

– Active Unit = RX
– Operation mode = Continuous

The D/A converter range is from +1023 to –1024 and the voltage range from 0.25v to 4.45 accurate to within 0,01v.



The value range of the error values is between –134 kHz and +134 kHz accurate to within 0.1 kHz.

If the measurement is incomplete when <Esc> is used, an information message is shown. The user can remove the information message with <Y>, <N> or <Esc> key. The measurement will be terminated by using <Y> key. The measurement will continue if <N> or <Esc> key is used.

Upon exiting, the next selections are set to the values which were selected before this adjustment.

– Active Unit
– Operation mode

Also AFC is set to the previous value.

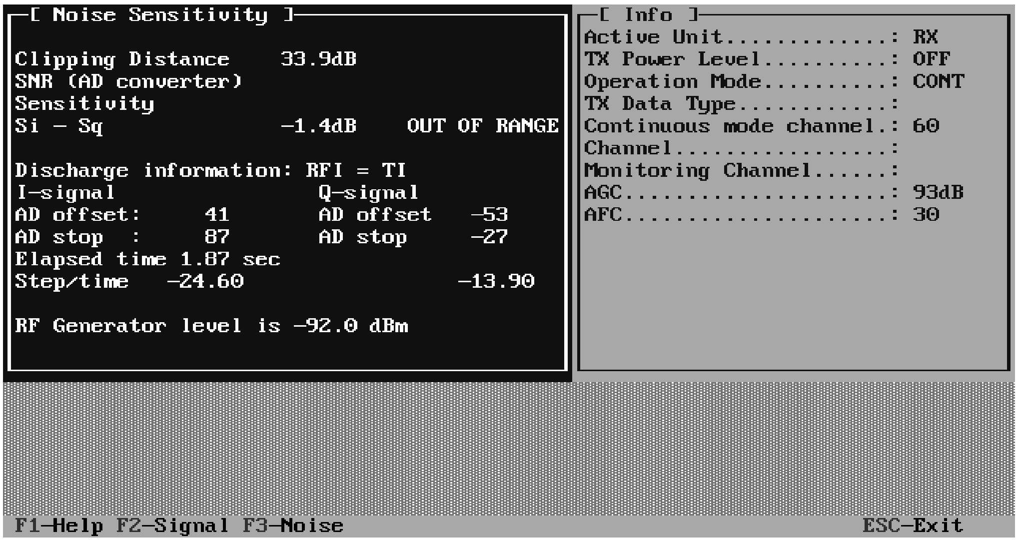
3.2.6 – Noise Sensitivity

This function is used for making Signal to Noise measurement.

The following automatic selections are made when this tuning function is activated:

– Active Unit = RX
– Operation mode = Continuous
– AGC = 93 dB in GSM ; 81dB in PCN

When this selection is made the next window is displayed.



Clipping distance is the difference to the signal clipping value. SNR is measured in the A/D converter.

Clipping distance = clipping level (66) – signal value + comp_factor1 SNR = signal value – noise value + comp_factor1

Sensitivity = –90 dBm + 8 dB + comp_factor2 – SNR

The last value on the display is signal power difference between I and Q branch. The numbers are shown in 0.1 dB accuracy. The error messages, ”OUT OF RANGE”, are shown only if the SNR and/or amplitude difference values are not acceptable.

(SNR <= 18 dB + comp_factor2 – 0.5 dB(=accuracy) ;
Sensitivity >= –100 dBm + 0.5 dB ; |Si – Sq| > 1dB).

When <F2> or <F3> is pressed, the RX I and Q burst data is asked for and ”SIGNAL MEASURING” or ”NOISE MEASURING” is displayed. The power level value should be –90 dBm during signal measurement.

Only the <Esc> key is accepted during measurement. <Esc> breaks the measurement routine in the PC and returns the program to the state before <F2> or <F3> was pressed. Normally <Esc> is not needed.

When signal data is received, the distance to clipping signal level is shown as dBs on the display. When either signal or noise measurement results are received ”MEASURING” text is removed and the first mentioned help line is on the display. When both measurements (signal and noise) are done at least once, the signal to noise relationship and difference are also shown on the display.

Upon exiting, the next selections are set to the values which were selected before this adjustment.

– Active Unit
– Operation mode
– AGC value

Compensation factors:

comp_factor1 = 4.64 dB (Compensation factor for 67.71 kHz signal, because ASIC filter attenuates 67.71 kHz signal 4.64 dB)

comp_factor2 = 2.27 dB (Compensation factor for real and calculated noise bandwidth difference. Real noise bandwidth is 80 kHz and calculated bandwidth is 135 kHz)

3.2.7 – Charge Voltage Adjustment

This function needs 6 V charge voltage from external power supply. When the function is activated the next window will be shown.

The A/D converter has positive 10 bit value.

The A/D converter value is read again when the previous value is received and shown on the screen.

If no measurement result is received when <Esc> key is used, the information message is shown. The user can remove the information message with <Y>, <N> or <Esc> key. The measurement will be terminated by using <Y> key. The measurement will continue if <N> or <Esc> key is used.

When at least one measurement is completed and <Esc> key is used, the user must answer the values saving question. If <Esc> key is used, the measurement is continued.

3.2.8 – Battery Voltage Adjustment

This function needs 6 V battery voltage from external power supply. When the function is activated the next window will be shown.

The operation is the same as in Charge Voltage calibration.

3.3 – Call Simulation

3.3.1 – TX Power Level

All power levels (GSM: 5...15 PCN: 0...10) can be selected. This updates the same parameter as TX Power Level in the RF Controls menu.

***Note** that TEST value cannot be selected. If TEST value was in use when Call simulation menu was selected, power level is changed to the smallest value.*

3.3.2 – Channel

This displays the normal operating RF channel number. Normal GSM channel numbers can be selected. The same channel is used both for transmission and receiving, this updates the same parameter as Channel in the RF Controls menu.

3.3.3 – Monitoring Channels

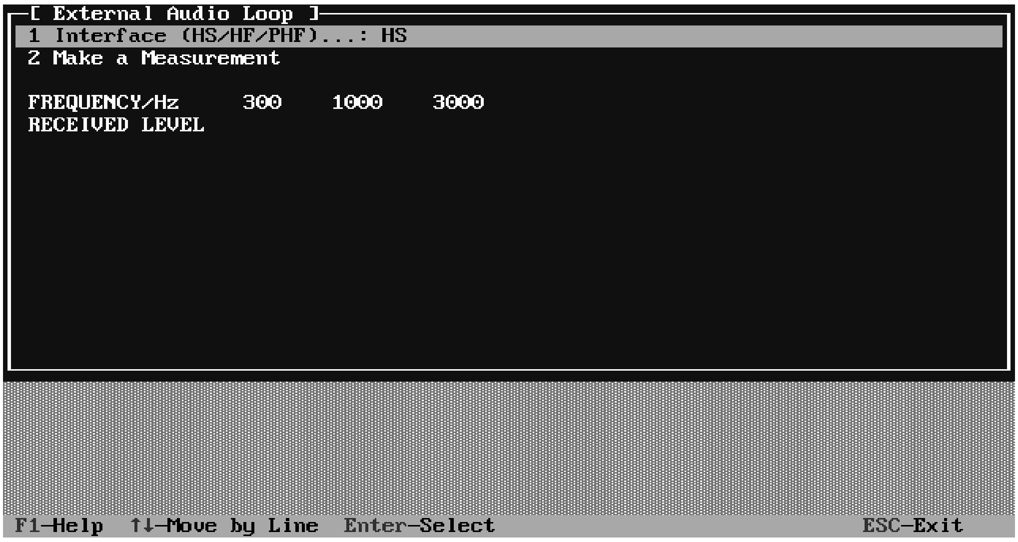
Channels for monitoring are specified with these six selections. All GSM channel numbers can be used. If more than one selection has the same number, the monitoring channel list (neighbour list) will have less than 6 selected channels. The minimum number of monitoring channels is one (all channels have the same value). The monitoring channel can also have same value as a normal operating channel. The first monitoring channel updates the same parameter as Monitoring Channel in the RF Controls menu.

3.4 – Internal Audio Loop

This test interface allows selection of input and output (Internal / External / Phf) and also connects and disconnects the test loop. The sent audio signal level has a constant value which depends on the selected interfaces.

When <Esc> key is used, the internal loop is automatically ended (Loop=Off).

3.5 – External Audio Loop



The first item selects the interface (Internal/External/Phf).

The sent audio signal level has a constant value which depends on the interface. When the frequency is changed, the received signal strength is measured and if too big an error message is displayed. Three different frequencies are used.

When Make a Measurement is selected, the received signal strength is displayed (square root of the received value) on the separate window. If any of the signal values differs more than ±3 dB from the reference values shown in the table below, the OUT OF RANGE message will be displayed.

	HS Interface		HF Interface		PHF Interface	
Freqncy	Ref value	Scale	Ref value	Scale	Ref value	Scale
300	25	15.....35	63	53.....73	63	53.....73
1000	32	22.....42	68	58.....78	68	58.....78
3000	32	22.....42	68	58......78	68	58.....78

Received level data fields have no value before measurement results are received. Below is the separate window where results are shown:

```
FREQUENCY/Hz      300    1000   3000
RECEIVED LEVEL    120     122    179   OUT OF RANGE
```

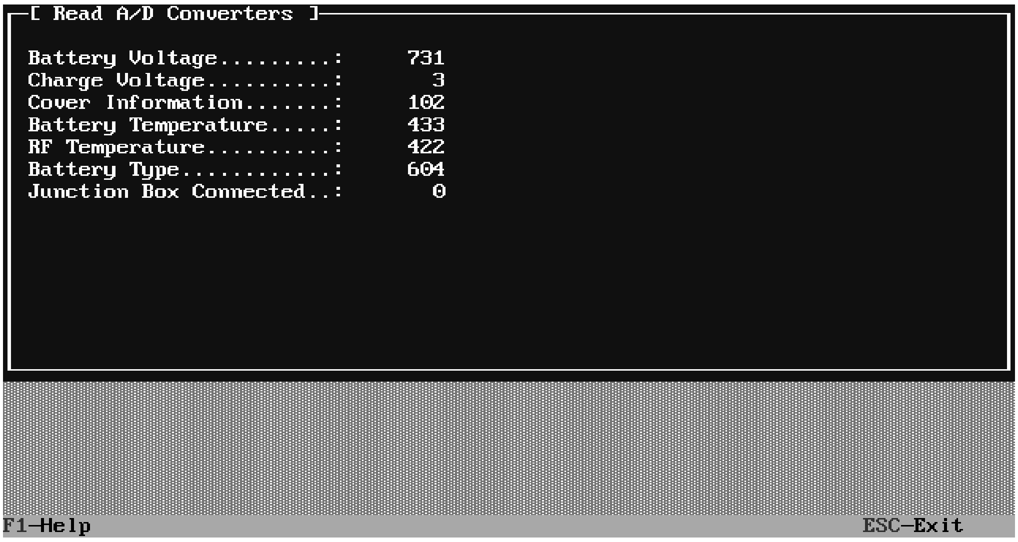
Received level value has scale from 0 to 256.

3.6 – Logic Controls

After this selection new window is shown:

3.6.1 – Read A/D Converters

After this selection new window is shown:



No value is shown when selected. When correspondent messages are received, the A/D converter values (10 bits decimal numbers) are displayed and read again. The exit is made with <Esc>.

3.6.3 – LCD Test Display

The LCD display is changed by using the number or <Enter> key. Two different test displays can be selected. When Logic Controls menu is selected, the display is controlled to the state shown in the menu.

– In test display 1 all indicators are displayed and the display is filled with chessboard letters.

– In test display 2 none of the indicators are displayed and the display is filled with inverse chessboard letters.

3.7 – MCU Selftests

When this selection is used, the user is informed

The phone will be set to the minimum mode

Y will run the special test mode and a reset will occur making MCU SW run only inside the MCU ROM code (=minimum mode). Also the test results that have been executed after last power–up will be asked from the phone.

N and ESC keys cancels the selection.

```
[ MCU Self-tests ]
1 Run Internal Test...........: OK
2 Run RAM BUS Test............: OK
3 Run ROM BUS Test............: OK
4 Run ROM Data Test...........: OK
5 Run ASIC BUS Test...........: NOT EXECUTED
6 Run ASIC Timer & IRQX Test...: NOT EXECUTED
7 Run ASIC Timer & NMI Test....: NOT EXECUTED
8 Run Audio Codec Test.........: NOT EXECUTED
9 Run RAM Component Test.......: NOT EXECUTED
A Run Ext. ROM Checksum Test...: NOT EXECUTED
B Run Display Driver Test......: NOT EXECUTED
C Run ASIC Type Test...........: NOT EXECUTED
D Run EEPROM Component Test....: NOT EXECUTED
E Run EEPROM BUS Test..........: NOT EXECUTED
F Run Software Reset Test......: NOT EXECUTED
G Run Power-off Test

F1-Help  F8-Bus Test                                  ESC-Exit
```

The test result will be shown to the user after each menu selection. If no response was received in the defined time, an error message is shown and ‘No Response’ text will be shown in the menu.

Note *power–off test (if passed) turns power off and power should be reconnected by using the phones keypad after the successful test. Power–off test works MCU internal SW Version 2.17 or higher.*

After the power has been connected to phone, the normal start–up routines are made and the self–tests results are shown in the MCU self–tests menu (i.e. all other than power–up self–tests are in NOT EXECUTED state after the power–up routines).

Test results will be one of the next: No Response, OK, NOT EXECUTED, FAILED. Note that power–off test have no values,because if test has been passed, power has been turned off. If power–off test fails a special error message window is shown.If no response is received to power off test message in a few seconds, the user is requested to turn the power on and press the return key.

3.8 – Set MCU Start–up Self–tests

This menu is used for changing the state of the EEPROM selectable tests. When selection is ”On”, the test will be run every time when automatic start–up self–tests are activated (e.g. in power–up).

When menu is selected, the previous values will be read from the MCU EEPROM and shown on the screen. When ESC is used, user is asked to confirm the EEPROM values saving. Error handling is done as in other functions which read and save EEPROM values.

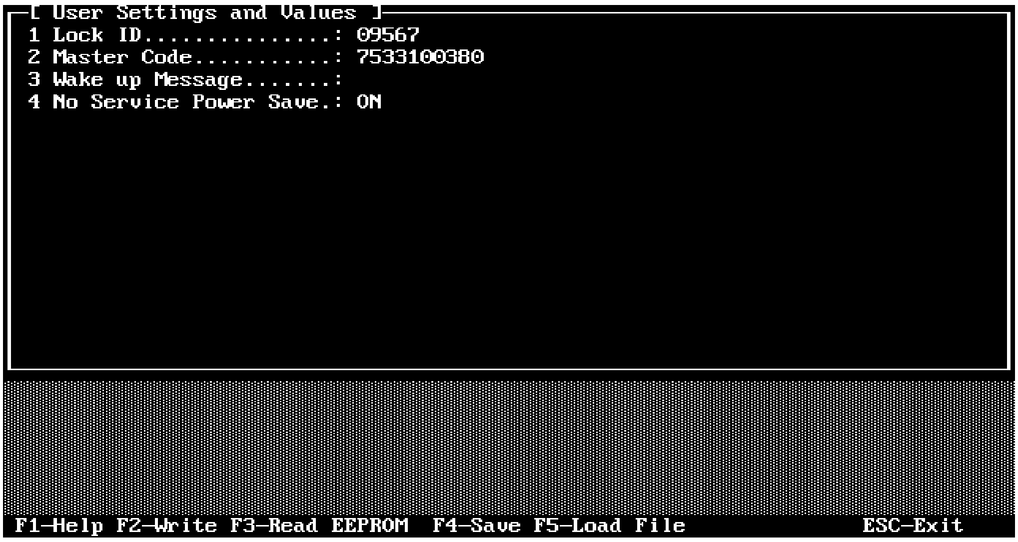
4 – ME Memory Functions

When ME Memory functions menu is selected the Phone Mode must be set to ‘Local’. If the local mode is not set, an error message is shown. Different parameters saved to the memory of ME can be read from memory or written to the memory.

When values to ME memory are saved, it asks for confirmation. If Y key is used, values are saved to the memory. If N or ESC key is used, the values are not saved to the memory.

4.1 – User Settings and Values

After this selection a new window is displayed.



4.1.1 – Lock ID

When this function is activated, the code can be edited; note that code is saved to the ME memory together with other user settings and values. Only digits are accepted for Security lock.

4.1.2 – Master Code

The master code cannot be edited.

4.1.3 – Wake Up Message

Examine the old Wakeup Message (read from the phone) or enter the new one.

4.1.4 – No Service Power

OFF: ”No Service Power Save” is not used.
ON: ”No Service Power” is used.

4.2 – Product Profile Settings

When Product Profile Settings selection is activated the Product Profile information is read from EEPROM. If the information is not received within 2 seconds an error message is shown and the ME Memory Functions menu is displayed. Otherwise the Product Profile Settings menu is displayed, where the user can select features.

When <Esc> key is used in this menu, the program will ask if the values are to be saved to the EEPROM or not. If <Y> key is used, values are saved to the EEPROM before the ME Memory Functions menu is displayed. If <N> key is used the ME Memory Functions menu is displayed without the save function being used. If <Esc> key is used the Product Profile Setting menu is shown and the values can be changed.

4.3 – Write HW Version

When HW version is selected, the current version is read from the phone and displayed.

4.4 – IMEI Edit

When this selection is made, the old IMEI is requested from EEPROM. If IMEI is not received within 2 seconds (approx.), an error message is displayed . Press any key to clear it and return to the previous menu.

If IMEI or EEPROM check sums have the wrong values, an error message is also displayed. After errors are acknowledged, the editing window is displayed without data, allowing at least 40 ASCII characters to be edited in the window. After IMEI data the password must be edited.

IMEI and password data are written to the EEPROM when editing is ended. The writing must be accepted by the user as with other EEPROM writing functions. If no response message from MCU to IMEI writing function is received within a few seconds, an error message is shown.

4.5 – IMEI Transfer

The purpose of this function is to transfer the IMEI code from an old system board to a new system board. This function is used when system boards are changed.

The selection, program asks to confirm the function with <Y> key. Pressing the <N> or <Esc> keys cancels the selection.

After pressing <Y> key the IMEI is read from EEPROM to PC. When the IMEI code is received by PC, information is displayed and the IMEI code is destroyed in the EEPROM. After clearing the IMEI number, the old system board becomes unusable.

Caution: The IMEI is now situated in the PC and quitting the Service software program at this stage will cause all IMEI data to be lost.

At this time, switch the phone power off, exchange the system boards and switch the phone power on again. A ”Selftest failed” –message will appear in the phones display.

After pressing the <Enter> key the IMEI will be transferred to the new system board. The IMEI data in the PC will be cleared and cannot be used again.

For resetting the phone you must select the ”Initialize phone” option from the ”Main menu”. If the phone does not show the ”Selftest failed”message, the transfer is successful. If the ‘fail’ message is still displayed, contact your local technical support .

4.6 – Set UI factory Values

This function sets the UI parameters to factory default values.

Phone mode must be in the Local mode when this menu is selected.

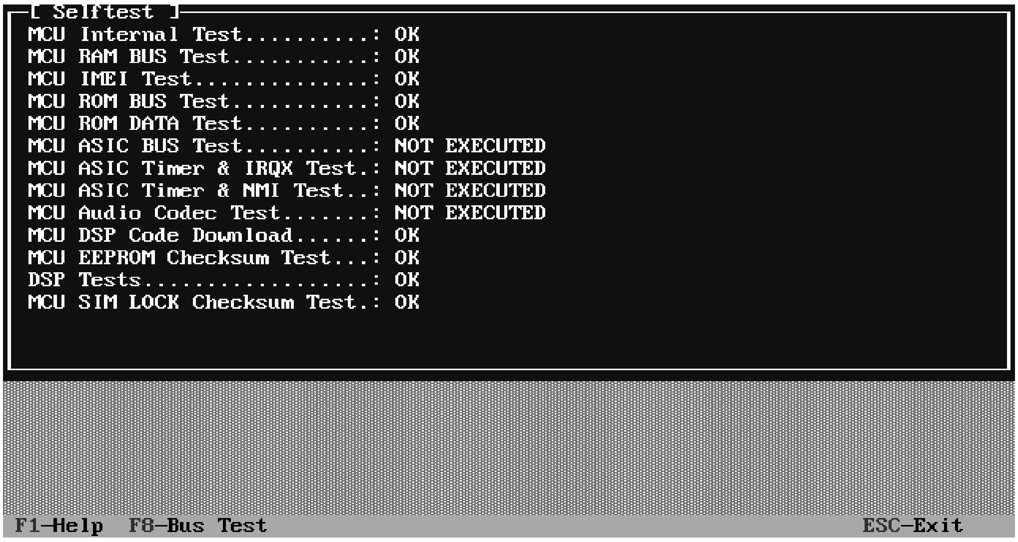
4.7 – Set Factory Values

The selection sets all except IMEI factory values (including UI). Even though no memory patch message is sent to mobile, the user is asked to confirm the functions with <Y> key.

***Note**: RF Tuning values are lost when this function is performed.*

5 – Power–up Selftests

This selection generates two windows:



When the window is activated, all test result fields have value ‘No response’. When responses are received, the values will be updated. When <Esc> key is used, the previous menu is displayed. Below is the list of DSP processor test faults. Only one fault value is indicated in the DSP processor selftest message. MCU test results are indicated one by one on the separate lines.

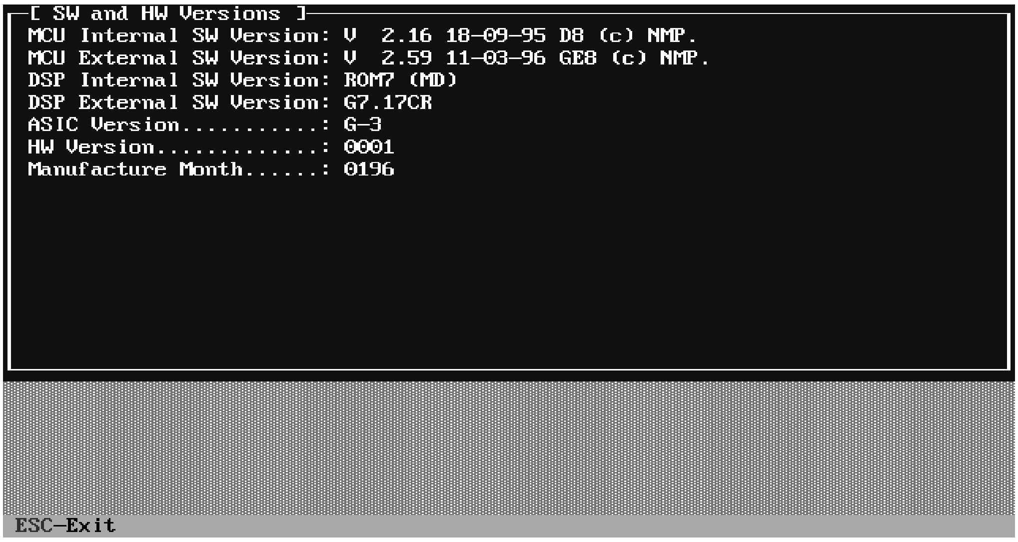
– RAM BUS Fault
– ASIC BUS Fault
– RFI BUS Fault
– Download Error

MCU test results will be one of the following: No Response, OK, NOT EXECUTED, FAILED

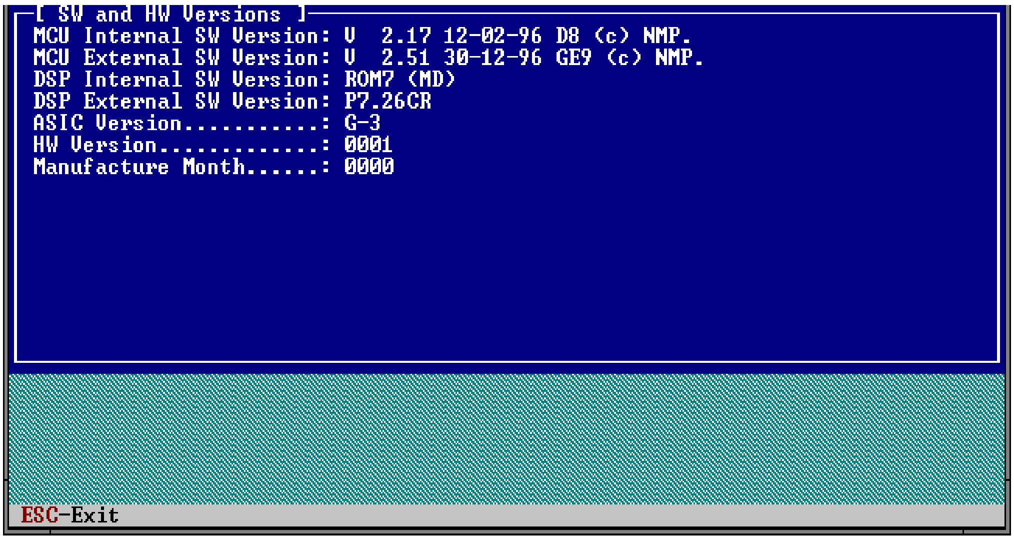
When <F8> key is pressed any failed test results are displayed. If no MCU BUS tests have failed, the display will say so. <Esc> key returns to the previous menu.

6. SW and HW Versions

This menu shows the current software and hardware versions.



GSM Version



PCN version

The next tuning window will be activated automatically after value selection. The power is presented in GSM values (5...15). The base GSM power (5) is selected automatically when the function is started. The test value is always the same when the function is started for the first time. The test value is not saved to the EEPROM and can be changed during tuning as other power coefficients and the program remembers its value when tuning function is activated later again.

If a SW version is not received, spaces are shown in that version number's place. The function is closed with <Esc> key.

7 – Phone Mode

With this function you can change the phone state (Normal or local mode).

When Normal mode is selected the normal start up functions take place in the phone and the phone is in normal operating mode.

When the local mode is selected the phone is deactivated to enable e.g. special RF tuning and adjustment values. These are requested from the phone and used to control hardware.

8 – PDA Commands See *PDA section*

9 – Faultlog

Faultlogger allows a complete service record to be built up from each phone repaired. The software automatically read the products details from EEPROM and writes a record to a pre–determined file. When an engineer adds the repair information, a complete service record is formed and this record can then be utilsed by database software for accurate fault reporting purposes

Basic Operating Principles

A valid ID and password is required to get access to faultlogger. When accepted, the unit to be repaired is connected to the software and the phones details are automatically read.

The repair is carried out and on completion of the repair, the work performed is entered manually on a data entry screen.

The automatic data, read earlier, is checked for validity. If O.K. the entry is saved and a complete service record is added to the fault log output file.

For further information refer to the *Faultlogger User's Guide for NHE–4*

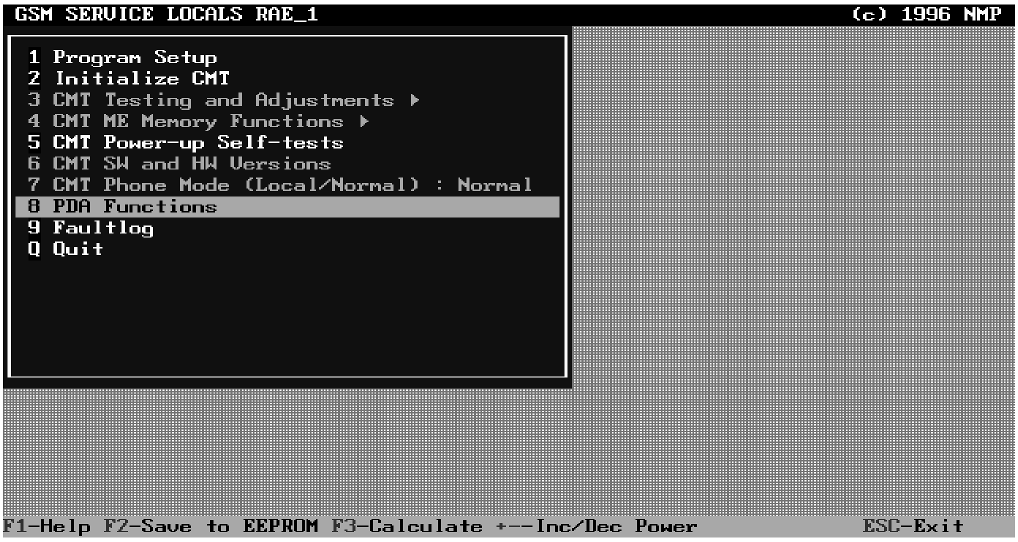
Q – Quit

This terminates the program and returns to DOS.

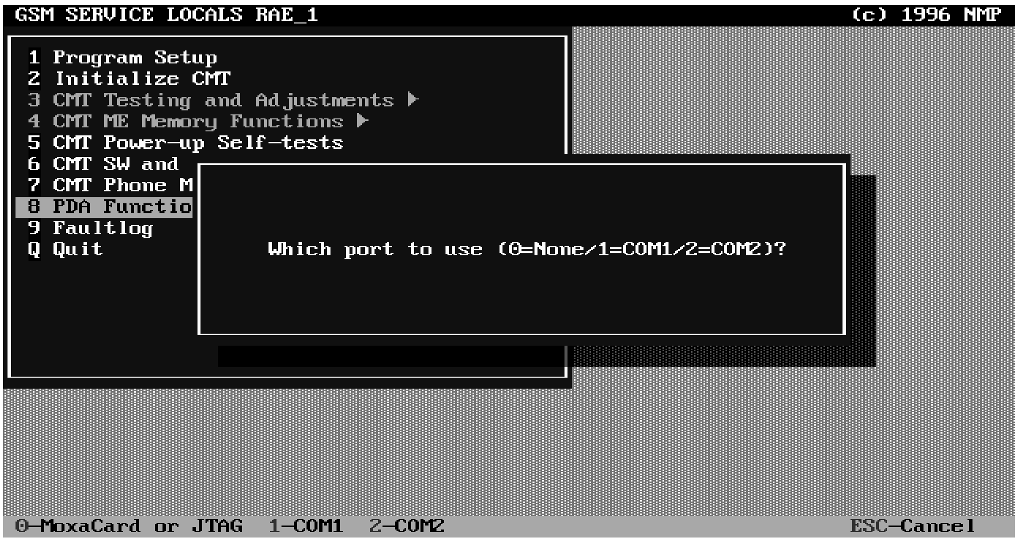
PDA Menu Commands

Introduction

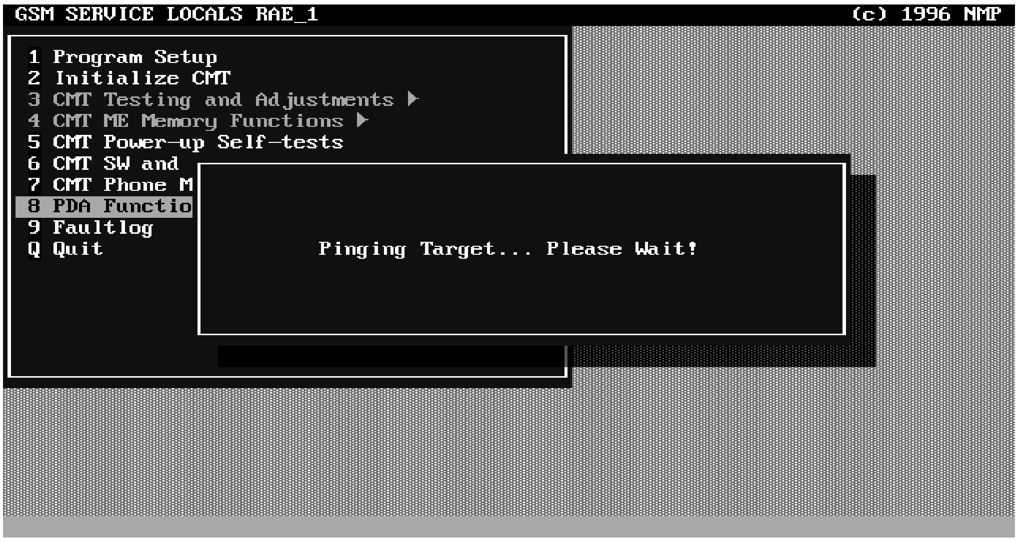
Upon selection, the service software will try to establish a communications link to the PDA module via the second serial port (if fitted) or alternatively when the DLR–1 connector is attached to the first serial port in place of the MBUS. Once a link is established between the service software and the PDA, further tests may be carried out.



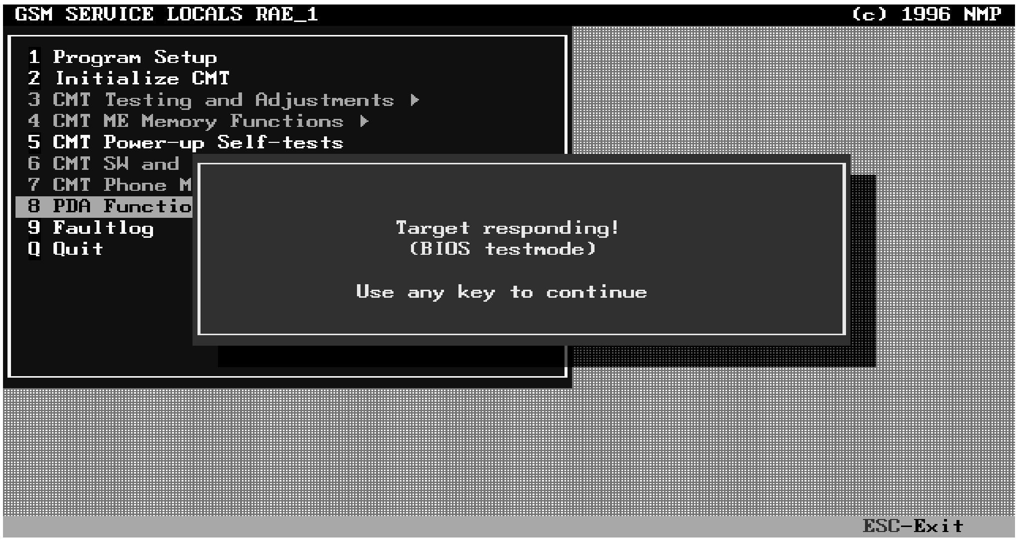
When ‘PDA Functions’ is selected, the serial port must be chosen, but before doing this , disconnect the power supply *(see note 1).



Select either **1** or **2** *(see note 2)and press enter to display the ‘Pinging Target’ message as shown overleaf.



At this point re–connect the power supply and a ‘Target responding’ message should be displayed as shown below.



NOTE 1 *This procedure is necessary in order for Pinging to function correctly.*

2 *If the default ’None’ is chosen, only the ’Flash Utilities,’Flash Several Targets’ and ’JTAG Flashing’ menus are enabled for use.*

1.– Initialisation

This menu provides functions to direct the target either to the BIOS or to the DOS– testmode. The speed of the communications channel may be changed and verification of communications channel validity is also possible.

This menu has the following Sub–menus:

1.1.– Ping Target

This menu item verifies the validity of the communications channel by sending a test message to the target. If the channel is fully functional, the target responds to the message request.

Note: *Any user options become highlighted once the menu item is selected, these can be changed by using the arrow keys*

1.2 – Set Serial Speed

This menu item provides means to change the speed of the serial channel used between the service software and the PDA. This function sets the speed of the UART in the PC running the service software, and the speed of the UART in the target.

User options are as follows:

BaudRate default: 115200	Optional rates:	1200	2400
		4800	9600
		19200	28800,
		57600	115200

1.3 – Boot Operating System

This menu item commands the target to boot the primary operating system, typically DOS.

1.4 – Reset Target

This menu item commands the target to jump unconditionally to the desired memory location. This allows jumping from the DOS–testmode to the BIOS–testmode. If testmode pin is active while polling it in BIOS, the handler in the BIOS–test program is entered and the BIOS–testmode is activated.

User options are as follows:

Address default: BIOS–testmode	range:BIOS–testmode
	PON
	0000:0000 – FFFF:FFFF

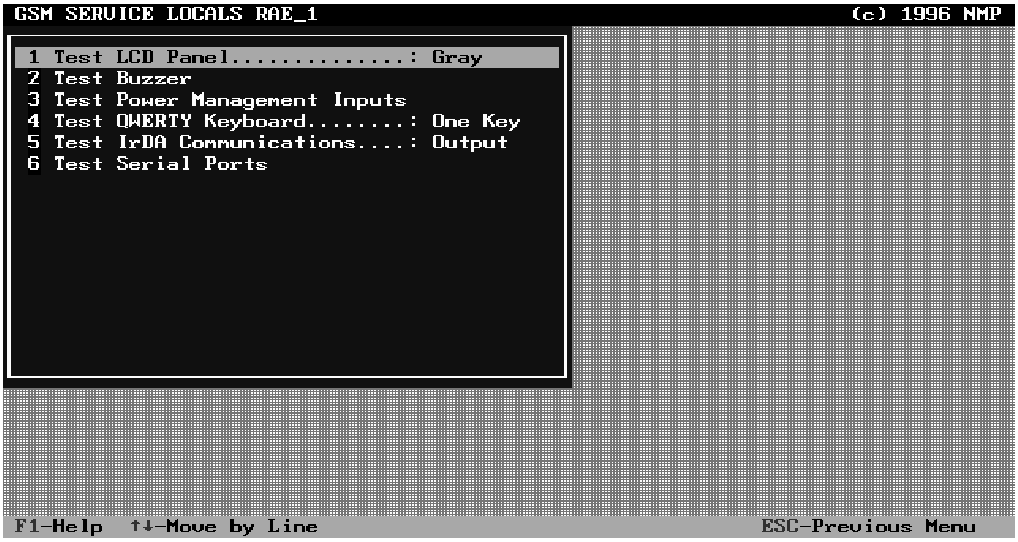
1.5 – Exit DOS–Testmode

This menu item commands the target to exit the DOS–testmode. i.e. if the menu is chosen, the secondary operating system, typically GEOS, is booted.

Note: *The GEOS looses the communications ability to the CMT if booted through either testmode. In this case, the GEOS will not operate normally.*

2 – Test Peripherals

This menu provides functions to test the discrete components of the PDA target.



2.1 – Test LCD Panel

This menu provides tests for the PDA LCD panel. Various test patterns can be chosen to be displayed with any contrast value.

User options are:

Contrast default:	128	range: 0 – 255	
Test Pattern default:	Gray	range:	Gray Gray inverted Matrix Matrix inverted Chess Chess inverted All ON All OFF Vision Vision inverted

2.2 – Test Buzzer

This menu provides a test for the PDA buzzer.

User options are:

Frequency default:	1000Hz	range:	20 – 18000Hz
Duration default:	1.0s	range:	0.1 – 25.5s

The input parameters are given as plain figures without units. Time referred input values are given as hundreds of milliseconds.

2.3 – Test Power Management Inputs

This menu provides a test for the PDA power management inputs.

The enquired input parameters from the user are:
TimeOut default: 5.0s range: 0.1 – 25.5s

The input parameters are given as plain figures without units. Time referred input values are given as hundreds of milliseconds.
PMI source is given as a result.

2.4 – Test QWERTY Keyboard

This menu provides tests for the PDA QWERTY keyboard.

User options are:

Method default:	One Key	Range:	One Key
TimeOut default:	25.5s	Range:	0.1 – 25.5s

The names of the pressed keys are displayed until the TimeOut measured from the last key pressed expires. If no key is pressed at all until within this timeout period the test is the TimeOut expires, considered to have failed.

To exit from the testing mode: press any key on the PC keyboard and then any key on the communicator.

2.5 – Test IR Communications

This menu provides a test for the PDA IR communications. One of the two methods to test the IR can be chosen. Test uses half–duplex method to test the input and the output capabilities of the target.

User options are:

Mode default: Output	range:	Output Input
Output Byte default: 55	range:	0 – FF(hex)

The IR tranceiver of the host PC will be set to the opposite port than that chosen for the service software, i.e. if the service software communications port is set to COM1, then the IR tranceiver will be connected to the COM2 and vice versa.

The IR speed defaults to the one used by the COM port for service software communications. The speed of the IR may be changed by changing the communications speed.

If the Mode is set to Output, the target sends the Output Byte via the target's IR transceiver. The same byte is expected to be able to be read via the the IR tranceiver connected to the service software PC. If the IR transceiver receives the Output byte, the test is considered successful.

If the Mode is set to Input, the target is commanded to wait for the Output Byte from the tranceiver connected to the service software. If the Output byte is received in the target, the test is considered successful.

2.6 – Test Serial Ports

This menu provides a test for the serial ports of the PDA. One of two methods to test one of the two COM ports can be chosen.

The enquired input parameters from the user are:

Mode default:	Local loop	Range:	Local loop
			External loop
Port default:	COM2	Range:	COM1
			COM2

If the Mode is set to Local loop, bytes from FFh to 0h are sent internally in the target's UART in a specific UART Local loop mode. If the same characters are received internally, the test is considered to been successful.

If the Mode is set to External loop, bytes from FFh to 0h are sent via the chosen COM Port of the target. The test expects the same bytes back via an external loop connected between RxD–TxD lines. Since the COM1 is used to the communications to the host service software PC, this mode cannot be used with the COM1.

3 – Flash Utilities see next section 'Flash Downloading'

4 – DRAM Utilities

This menu provides functions to access the PDA DRAM.

4.1 – Test DRAM

This menu provides a test utility for testing the PDA DRAM.

User options are:
Test type default: WalkingBit Range: WalkingBit
ChessBoard

Start Address default: 000000h Range: 000000 – 1FFFFFh

End Address default: 0FFFFFh Range: 3A00000h. – 1FFFFFh

The area between addresses B0000h – FFFFFh cannot be tested.

The output from the target shows the following:

whether the test was successful

4.2 – Read DRAM

This menu provides means to read the DRAM of the target.

User options are:

Start Address default: 000000h Range: 000000 – 1FFFFFh

The output from the target shows the following:

Values of the memory bytes at the enquired addresses

4.3 – Write DRAM

This menu provides means to write the DRAM of the target.

User options are:

Start Address default: 000000h	Range: 000000 – 1FFFFFh
Bytes default: none	Range: 0 – FFh

***Note**: The number of bytes has to be even*

5 – I/O Space Functions

This menu provides functions to access the PDA I/O Ports.

5.1 – Get Post CheckPoint

With this menu it is possible to read the last checkpoint written by BIOS during POST.

The output from the target shows the following:

the last POST checkpoint

5.2 – Read I/O Port

This menu allows the user to read any I/O port byte– or wordwise.

User options are:

Port Address default: none	Range: 0000h – FFFFh
Notation default: Byte	Range: Byte | Word

The output from the target shows the following:

Byte | Word in the enquired I/O port

5.3 – Write I/O Port

This menu allows the user to write any I/O port byte –or wordwise.

User options are:

Port Address default: none		Range: 0000h – FFFFh
Notation default:	Byte	Range: Byte | word
Byte default:	none	Range: 00h – FFh
Word default:	none	Range: 0000h – FFFFh

The output from the target shows the following:

Byte | Word in the enquired I/O port after writing it

5.4 – Get Date & Time

This menu reads the current date and time stored in the RTC CMOS memory.

The output from the target shows the following:

Current date and time stored in the RTC

5.5 – Set Date & Time

This menu allows the user to set the date and the time to the RTC CMOS memory.

User options are:

Date default: none	Range:	formatted DD.MM.YYYY
Time default: none	Range:	formatted HH.MM.SS

The output from the target shows the following:

Current date and time stored in the RTC

5.6 – Calculate CheckSum

By choosing this menu, the target calculates a 32–bit checksum of the ROM between given physical addresses. If a ready calculated checksum is given as a input, it is compared to the one to be calculated. If the input checksum equals to zero no comparison is made.

User options are:

Start Physical Address default:3C00000h	Range:	3A00000h 3C00000h 3E00000h
Start Relative Address default: 000000h	Range:	000000h – 1FFFFFh
End Physical Address default: 3E00000h	Range:	3A00000h – 3C00000h 3E00000h
End Relative Address default: 1FFBFFh	Range:	000000h – 1FFFFFh
Checksum to compare default:00000000h	Range:	00000000h – FFFFFFFFh

The output from the target shows the following:

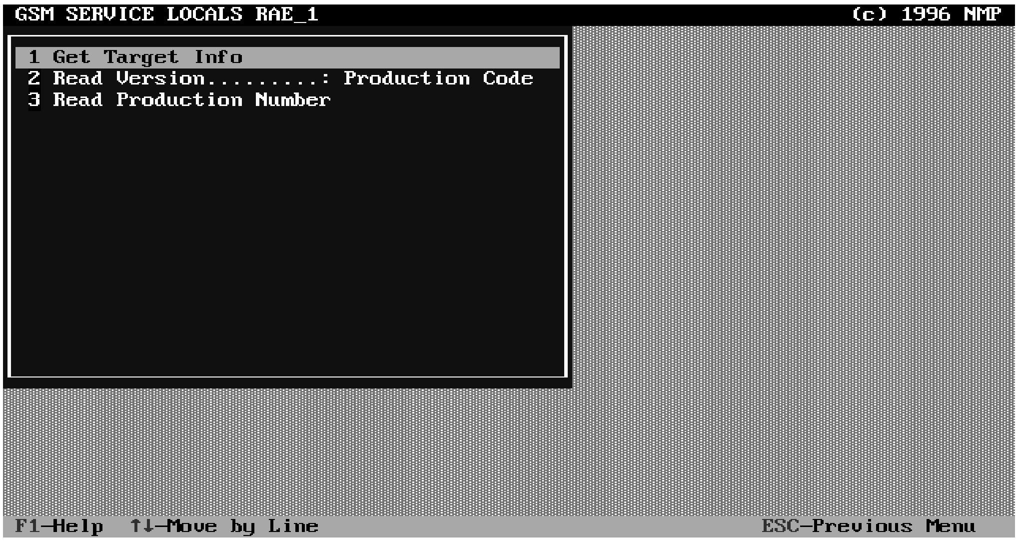
Calculated 32–bit checksum
whether the checksums are equal

5.7 – Target DOSshell

By choosing this menu, the user can write a command that will be executed in the target’s DOS.

6 – Product Information

This menu provides functions to access the production– and the service information of the PDA.



6.1 – Get Target Info

This menu shows additional information of the target itself. All the information is not necessarily supported by both TestModes.

6.2 – Read Version

This menu returns either the Production Code, Hardware version or the Software version of the target.

User options are:

Name default: Production Code	Range:	Production Code Hardware Software

The output from the target shows the following:

The enquired information

6.3 – Read Production Number

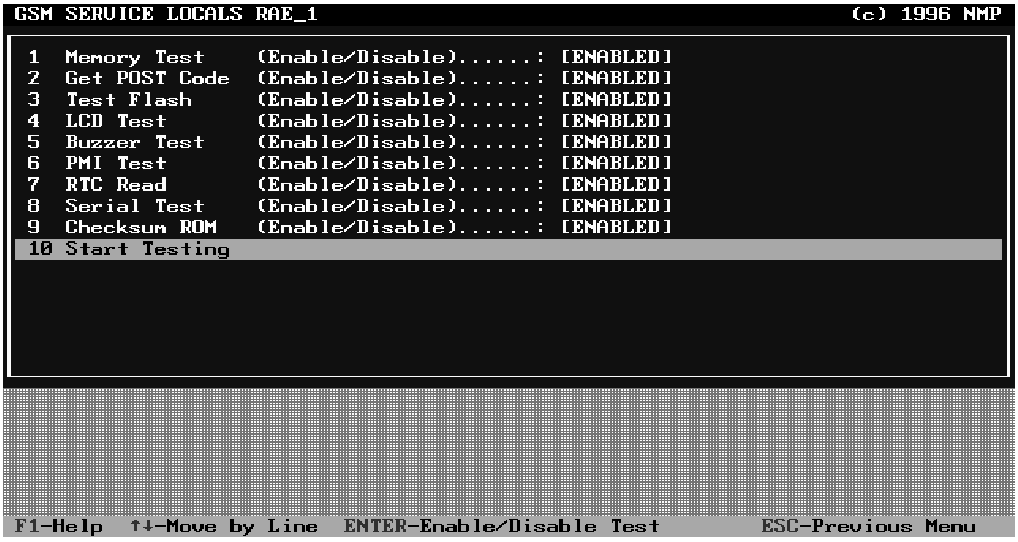
This menu returns the Production Number.

The output from the target shows the following:

The production number

7 – Complete Test

This menu provides functions to perform various test with default parameters automatically. Any of 9 different tests maybe included or excluded to the test series. Choosing the ’Start Testing’ starts the automatic test sequence.



7.1 – Memory Test

Enabling this choice adds the memory test to be included to the test sequence. The test is performed with default parameters.

The default parameters used:

Test type default: chessboard

Start address default: 000000h

End address default: 0AFFFFh

The output from the target shows the following:

whether the command was parsed succesfully
whether the test was succesful

7.2 – Get POST Code

Enabling this choice adds the POST code read to be included to the test sequence. The test is performed with default parameters.

The default parameters used: none

The output from the target shows the following:

whether the command was parsed successfully
whether the test was successful

7.3 – Test Flash

Enabling this choice adds the Flash test to be included to the test sequence. The first block of each Flash device is checksummed, then it's read and saved on a disk in the service software. After the block is saved, the physical block is erased, and then programmed from the file where the contents was saved.

After programming, the block is checksummed and the result is compared to the original one. If the checksums are equal with each block, the test is considered successful. The test is performed with the default parameters shown below:

Filename	default:Flashtest.bin
Start Physical Address	default:3A00000h
Start Relative Address	default:000000h
End Physical Address	default:3A00000h
End Relative Address	default:00FFFFh
Start Physical Address	default:3C00000h
Start Relative Address	default:000000h
End Physical Address	default:3C00000h
End Relative Address	default:00FFFFh
Start Physical Address	default:3E00000h
Start Relative Address	default:000000h
End Physical Address	default:3E00000h
End Relative Address	default:00FFFFh

The output from the target shows the following:

whether the test was successful

7.4 – LCD Test

Enabling this choice adds the LCD test to be included to the test sequence. The test is performed with default parameters as follows:

Contrast default:	128
Test Pattern default:	Gray
	Gray inverted
	Matrix
	Matrix inverted
	Chess
	Chess inverted
	All ON
	All OFF
	Vision
	Vision inverted

7.5 – Buzzer Test

Enabling this choice adds the Buzzer test to be included to the test sequence. The test is performed with default parameters as follows:

Frequency default:	500 Hz
Duration default:	0.3 s
Frequency default:	1000 Hz
Duration default:	0.3 s
Frequency default:	1500 Hz
Duration default:	0.3 s

7.6 – PMI Test

Enabling this choice adds the PMI test to be included to the test sequence. The test is performed with default parameter. This test requires user activity; the user must turn the CMT module on/off using the CMT power switch, or/and the user must open/close the UI.

The default parameters used:
TimeOut default: 25.0 s

The output from the target shows the following:

whether the test was successful

7.7 – RTC Test

Enabling this choice adds the RTC test to be included to the test sequence. The test is performed with no default parameters.

The output from the target shows the following:

whether the test was successful

7.8 – Serial Test

Enabling this menu adds the Serial test to be included to the test sequence. The test is performed with default parameters as follows:

Mode default:	Local loop
Port default:	COM1
	COM2

The output from the target shows the following:

whether the test was successful

7.9 – Checksum ROM

Enabling this choice adds the Checksum ROM test to be included to the test sequence. The test is performed with default parameters as follows:

Start Physical Address	default:3C00000h
Start Relative Address	default: 000000h
End Physical Address	default:3E00000h
End Relative Address	default: 1FFBFFh

The output from the target shows the following:

whether the command was parsed successfully
whether the test was successful

7.10 – Start Testing

Choosing this choice, the automatic test sequence is started using the enabled tests. These tests can be carried out individually by disabling all tests except the one required and then selecting ‘Start Testing.’

The output from the target shows the following:

whether the tests are O.K. or have failed.

Flash Downloading

GP1 (PDA) module Flash image can be downloaded two ways. The most common way is to use RS232 cable DLR–1, and a modified Power Adapter module. This Flash downloading can be done either one communicator at a time or simultaneously for eight communicators.

The JTAG method is required if the uppermost flash device in the memory map (D163, schematic reference) is changed to a blank flash device.   In this method a special adapter card is connected to the dummy test battery.

GE8 (CMT) module Flash image is downloaded using Flash Programming Set FPS–3. The dummy test battery is needed in addition to ordinary FPS–3 hardware and software.

Flash image download setups for both modules is illustrated overleaf.

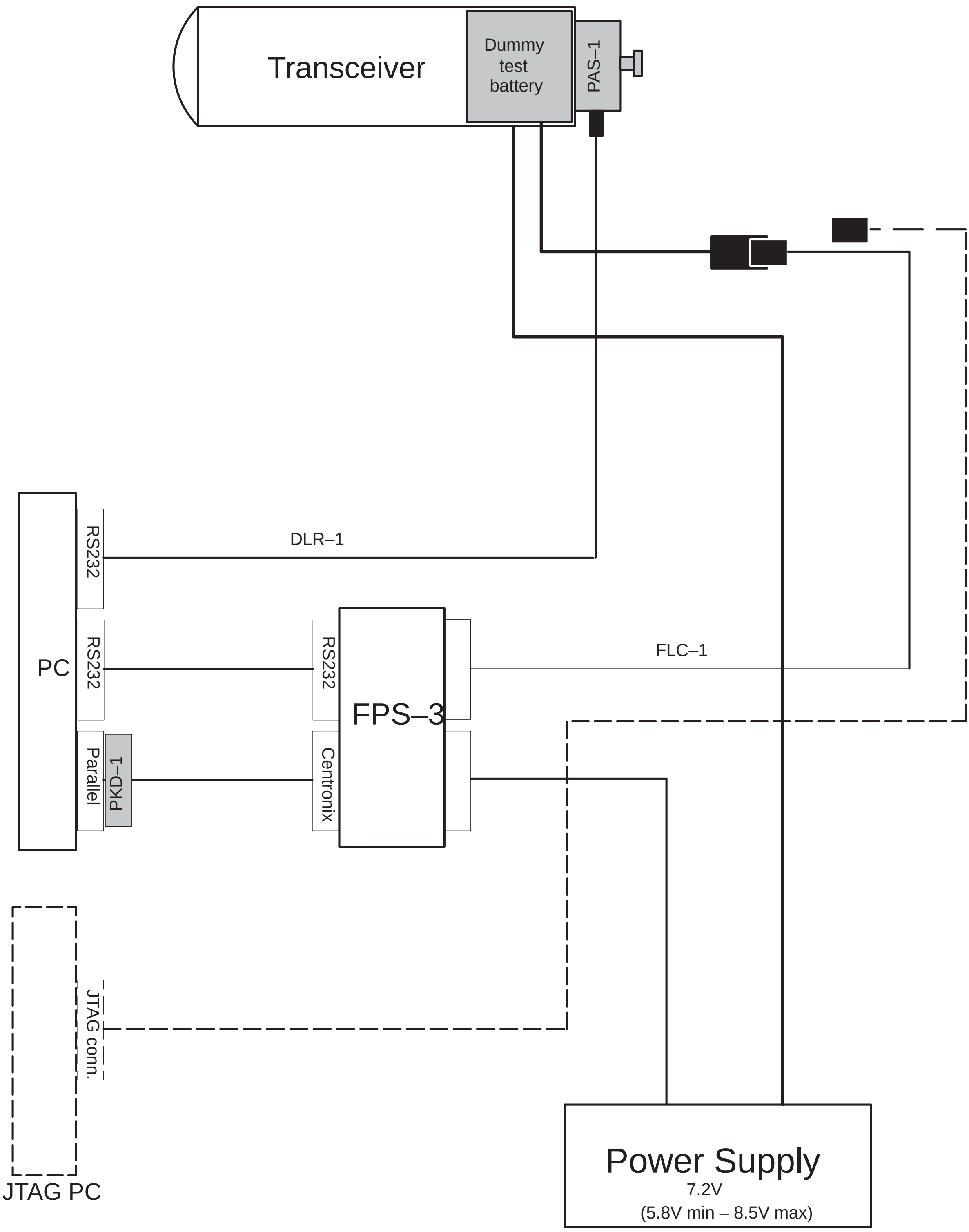
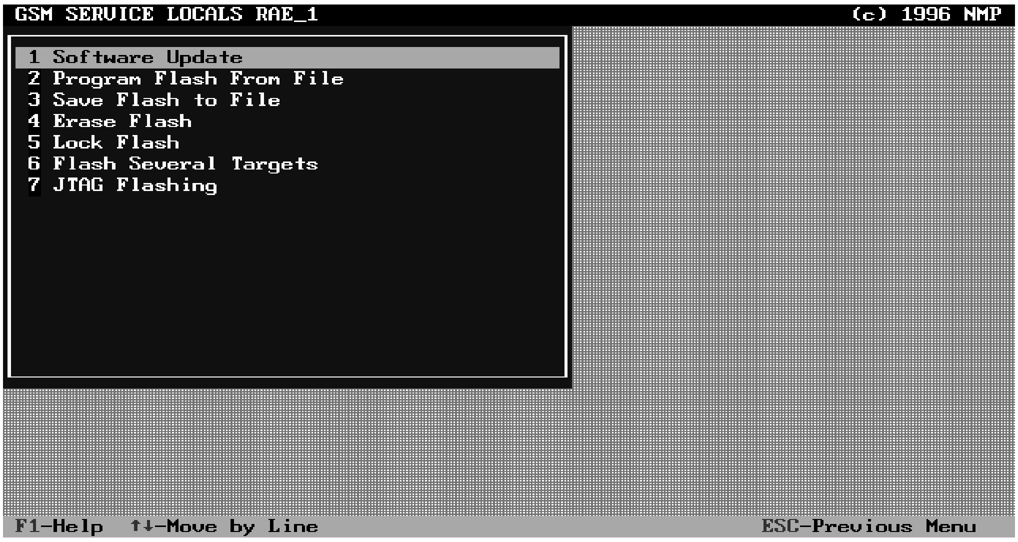


Figure 3. GE8 and GP1 FLASH Download connections. JTAG PC is backup method for GP1 FLASH download.

3. – Flash Utilities

This menu provides functions to access the PDA Flash memory.



3.1 – Software Update

This menu provides means to update the software in the PDA's Flash memory from a file on the disk in the host. The user is expected to give the Name of the Update, i.e. the name of the image file that will be programmed to the Flash memory of the target PDA. The name of the file must be given without extension. The service software gets the extensions of the header file and the image file from the PDA initialization file.

The Software Update reads the image file, sends it to the target in blocks, erases the needed blocks of the Flash, programs them and locks them. After the image is programmed, the updated memory area is check–summed and the result is compared to the one given in the header file. The memory area between 3FFFC00h – 3FFFFFFh is not included to the area, where the checksumming is done.

The output from the target shows the following:
whether the buffer filling was successful
whether the Flash erasing was successful
whether the Flash programming was successful
whether the Flash locking was successful
whether the Flash check summing was successful

8 **3.2 – Program Flash from File**

This menu provides means to program the PDA Flash memory from a file on the disk in the host.

Start Physical Address default: 3C00000h range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h range: 000000h – 1FFFFFh

If the Start Physical Address is set to 3E00000h the maximum Start Relative Address may not be greater than 1FFBFFh.

The output from the target shows the following:
whether the buffer filling was successful
whether the Flash programming was successful

3.3 – Save Flash to File

This menu provides means to read contents of Flash memory and to save it to a file in the host service software PC.

User options are:

Start Physical Address default: 3C00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

End Physical Address default: 3E00000h Range: 3A00000h
3C00000h
3E00000h

End Relative Address default: 1FFFFFh Range: 000000h – 1FFFFFh

The output from the target shows the following:
whether the command was parsed successfully
whether the Flash reading to buffer has been successful
whether the transferring of the buffer contents has been successful.

3.4 – Erase Flash

This menu provides means to erase one or more blocks of the PDA Flash memory.

User options are:

Start Physical Address default: 3A00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

End Physical Address default: 3A00000h Range: 3A00000h
3C00000h
3E00000h

End Relative Address default: 1FFFFFh Range: 000000h – 1FFFFFh

The output from the target shows the following:
whether the command was parsed successfully
whether the Flash erasing has been successful

3.5 – Lock Flash

This menu provides means to lock one or more blocks of the PDA Flash memory. This function sets the particular lock bit in each Flash memory block that is to be locked.

User options are:

Start Physical Address default: 3C00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

End Physical Address default: 3E00000h Range: 3A00000h
3C00000h
3E00000h

End Relative Address default: 1FFFFFh Range: 000000h – 1FFFFFh

The output from the target shows the following:
whether the command was parsed successfully
whether the Flash locking has been successful

3.6 – Flash Several Targets

This menu provides functions to access the PDA Flash memory.

3.6.1 – Ping Targets

This menu item verifies the validity of the communications channels to all the targets that the external serial ports card supports, by sending a test message to the targets. If the channels are fully functional, the targets respond to the message requests.

The pinging can be repeated as soon as the other required targets have replied. The user will not have time to boot up all eight targets all at once.

The output from the target shows the following:

how many targets responded

3.6.2 – Software Update

This menu provides means to update the PDA Flash memory in parallel to all the targets from a file on the disk in the host. The enquired input parameters from the user are:

Name of the Update	default:	none	range:	none

The user is expected to give the Name of the Update, i.e. the name of the image file that will be programmed to the Flash memories of the target PDAs. The name of the file must be given without extension.

The service software gets the extensions of the header file and the image file from the PDA initialization file. The Software Update reads the image file, sends it to the targets in blocks, erases the needed blocks of the Flash, programs them and locks them.

After the image is programmed, the updated memory area is checksummed and the result is compared to the one given in the header file. The memory area between 3FFFC00h – 3FFFFFFh is not included in the area where the checksumming is done.

3.6.3 – Erase Flash

This menu provides means to erase one or more blocks of the PDA Flash memory in parallel to all the targets.

User options are:

Start Physical Address default: 3A00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

End Physical Address default: 3A00000h Range: 3A00000h
3C00000h
3E00000h

End Relative Address default: 1FFFFFh Range: 000000h – 1FFFFFh

The output from the target shows the following:

whether the command was parsed successfully
whether the Flash erasing has been successful

3.6.4 – Lock Flash

This menu provides means to lock one or more blocks of the PDA Flash memory in parallel to all targets.

User options are:

Start Physical Address default: 3C00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

End Physical Address default: 3E00000h Range: 3A00000h
3C00000h
3E00000h

End Relative Address default: 1FFFFFh Range: 000000h – 1FFFFFh

The output from the target shows the following:

whether the command was parsed successfully
whether the Flash locking has been successful

3.6.5 – Program Flash From File

This menu provides means to program the PDA Flash memory from a file on the disk in the host to all the targets in parallel.

Start Physical Address default: 3C00000h Range: 3A00000h
3C00000h
3E00000h

Start Relative Address default: 000000h Range: 000000h – 1FFFFFh

If the Start Physical Address is set to 3E00000h the maximum Start Relative Address may not be greater than 1FFBFFh

The output from the target shows the following:

whether the command was parsed successfully
whether the buffer filling was successful
whether the Flash programming was successful

3.6.6 – Calculate Checksum

By choosing this menu, the target calculates a 32–bit checksum of the ROM between the given physical addresses.

User options are:

Start Physical Address default: 3C00000h Range: 3A00000h
3FFFBFFh

End Physical Address default: 3FFFBFFh Range: 3A00000h
3FFFBFFh

The output from the target shows the following:

whether the commands were parsed successfully
Calculated 32–bit checksum

3.7 – JTAG Flashing

This menu provides means to program the PDA Flash memory from a file on the disk using the JTAG interface of the target.

The output from the target shows the following:

whether the command was parsed successfully
whether the commands in the configuration file were executed successfully

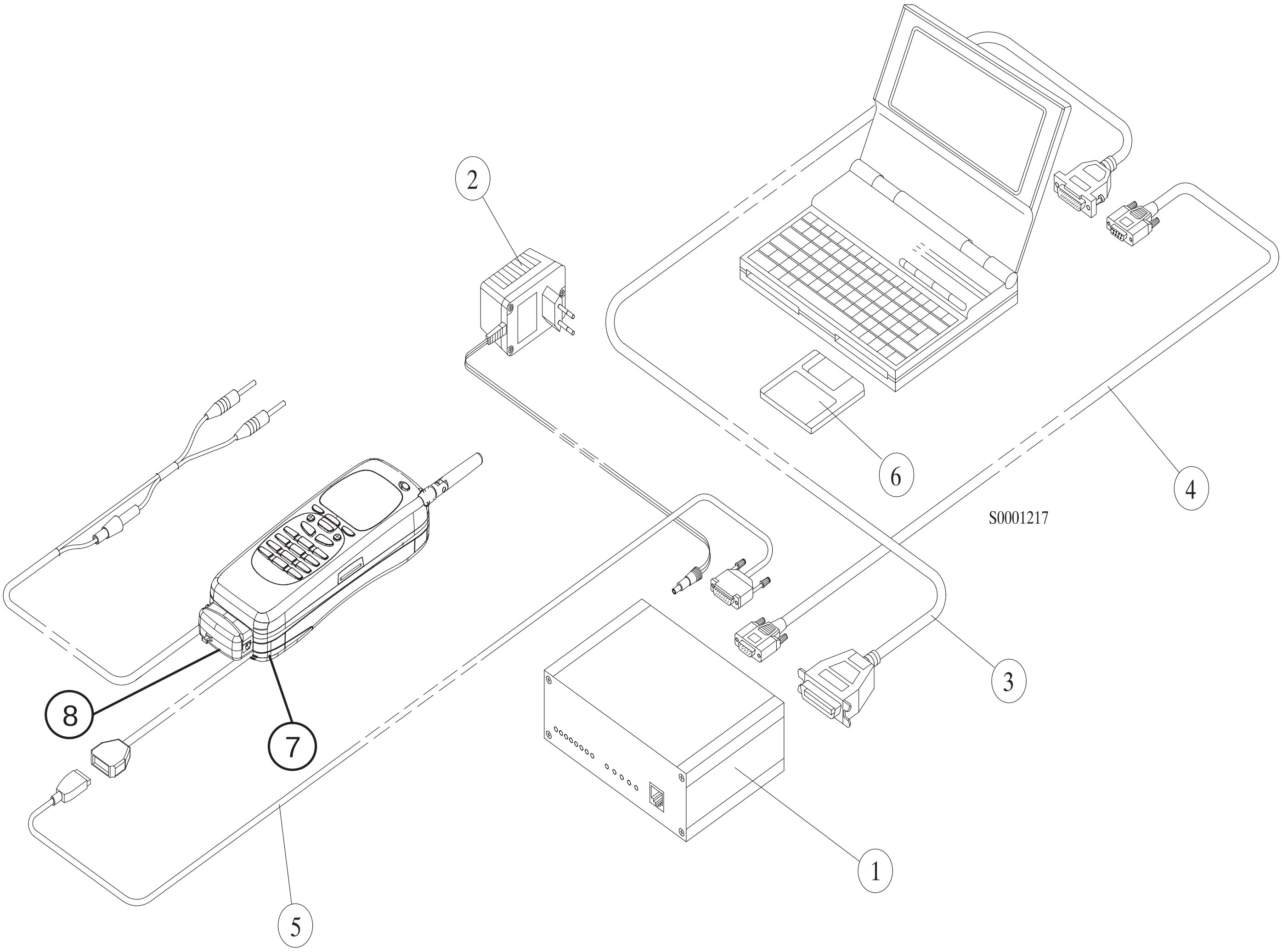


Figure 4. CMT Upgrading Software Setup

1. FPS–3 PROGRAMMER
2. ACS –X POWER SUPPLY
3. FPS–3 –CABLE
4. FPS–3 –CABLE
5. FPS–3 –CABLE
6. SERVICE SOFTWARE DISK X 2
7. BTD–1 TEST BATTERY
8. PAS–1 MODIFIED POWER ADAPTER

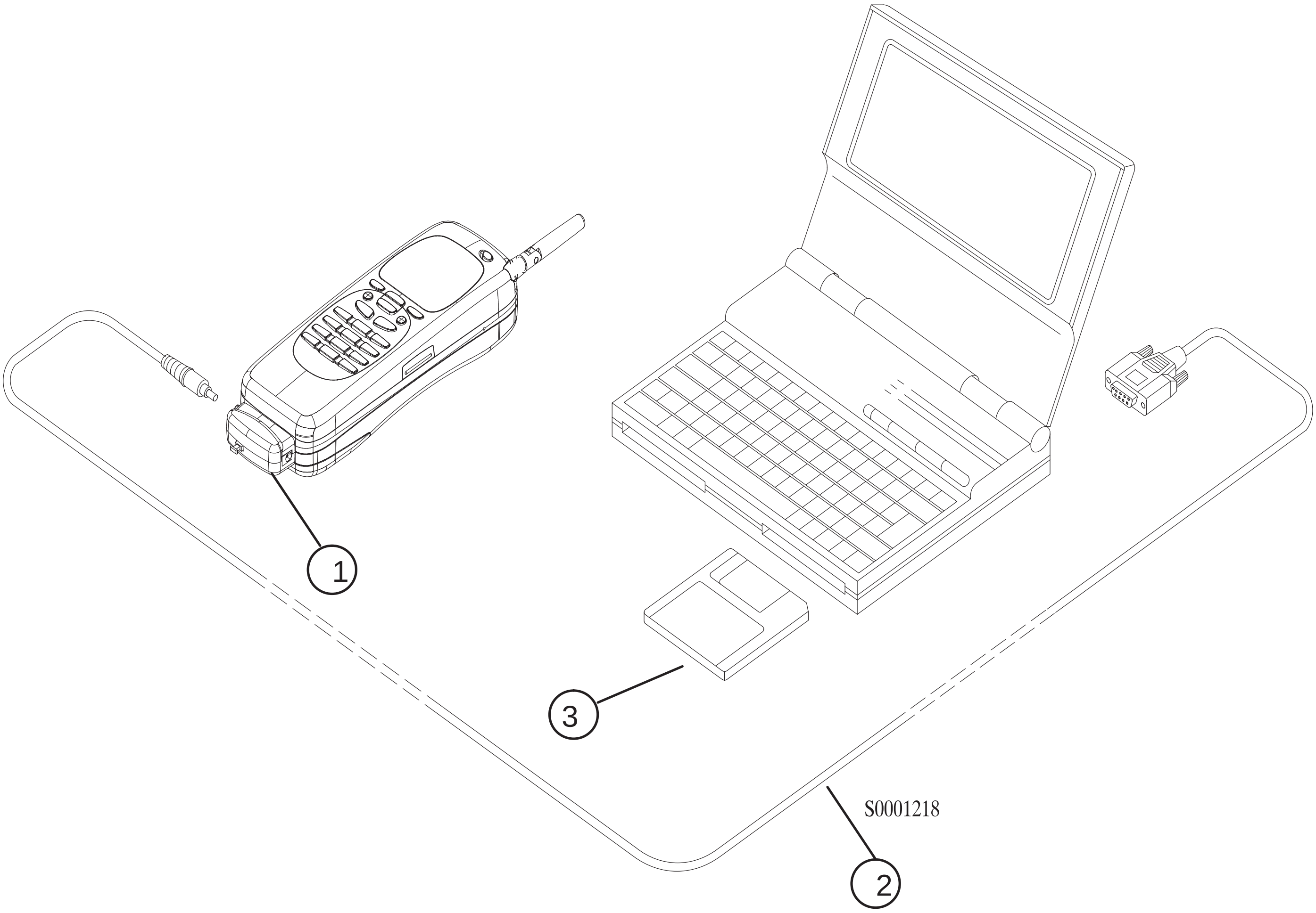


Figure 5. PDA Upgrading Software Setup

1. PAS–1
2. DLR–1
3. SERVICE SOFTWARE 3”DISK X 2

Tuning Instructions

General

The service software program turns the phone into Locals mode, which controls the phone via the M2BUS interface.

Tuning is based on the software communicating with the D/A and A/D converters of the phone. In some instances the phone processor will also calculate the required correction parameter.

The tuning values of the phone reside on the EEPROM. The program enables writing the default parameters on the EEPROM, in which case all tuning steps should be carried out.

NOTE. *During tuning, proceed as follows:*

– Take care not to damage sensitive measuring instruments with excessive RF power.

– Carry out all tuning steps in the shortest possible time to avoid excessive heating of RF units.

– Perform all tuning steps in the order presented.

– Never try to mask a fault by tuning it out!

Required Equipment

– PC/AT computer with service software software; see Sect. 7 for instructions on installation and use.

– M2BUS adapter DAU–2 and other service accessories; see equipment setup pictures.

– Multimeter or DVM.

– GSM radio telephone test station or separate measuring equipment as follows:

  – frequency counter (±1 ppm)

  – RF generator

  – pulse power meter

  – spectrum analyzer

  – attenuator and branching unit

Equipment Setup

To set up the equipment, connect the M2BUS adapter to the serial port (RS–232) of the computer. In case you are using a 9–pin serial port (normal with an AT set) use the mating adapter supplied with the M2BUS adapter. Turn off the computer before connecting to avoid possible damage to the serial port.

Attach one end of the XCM–1 modular cable to the DAU–2 PC/M2BUS adapter and the other end to the modulator T–connector when the covers of the phone are in place.

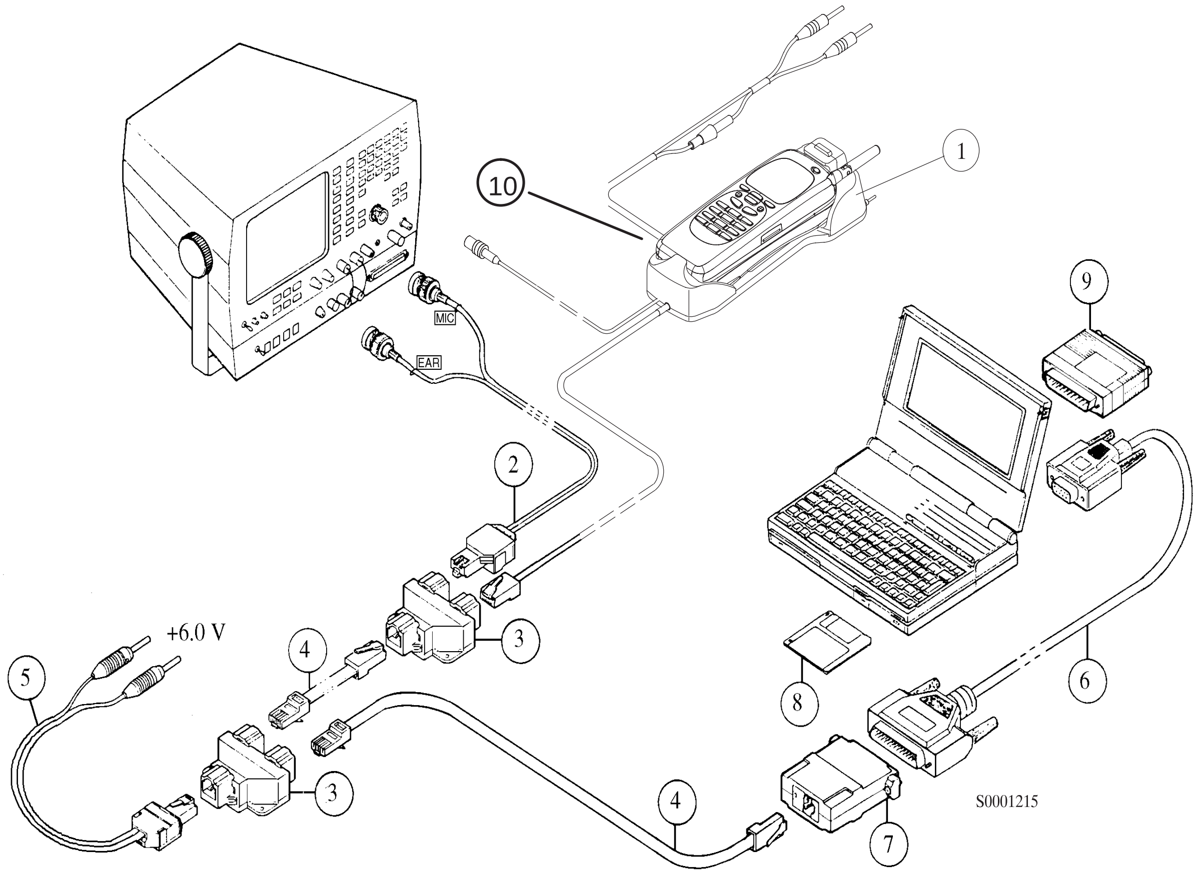


Figure 6. Tuning setup, with covers on

1. HCR–1
2. ADS–1
3. MODULAR T CONNECTOR
4. XCM–1
5. SCF–6
6. RS232 9–25 PIN ADAPTER
7. DAU–2
8. SERVICE SOFTWARE 3”DISK
9. PKD–1 DONGLE
10. BTD–1C

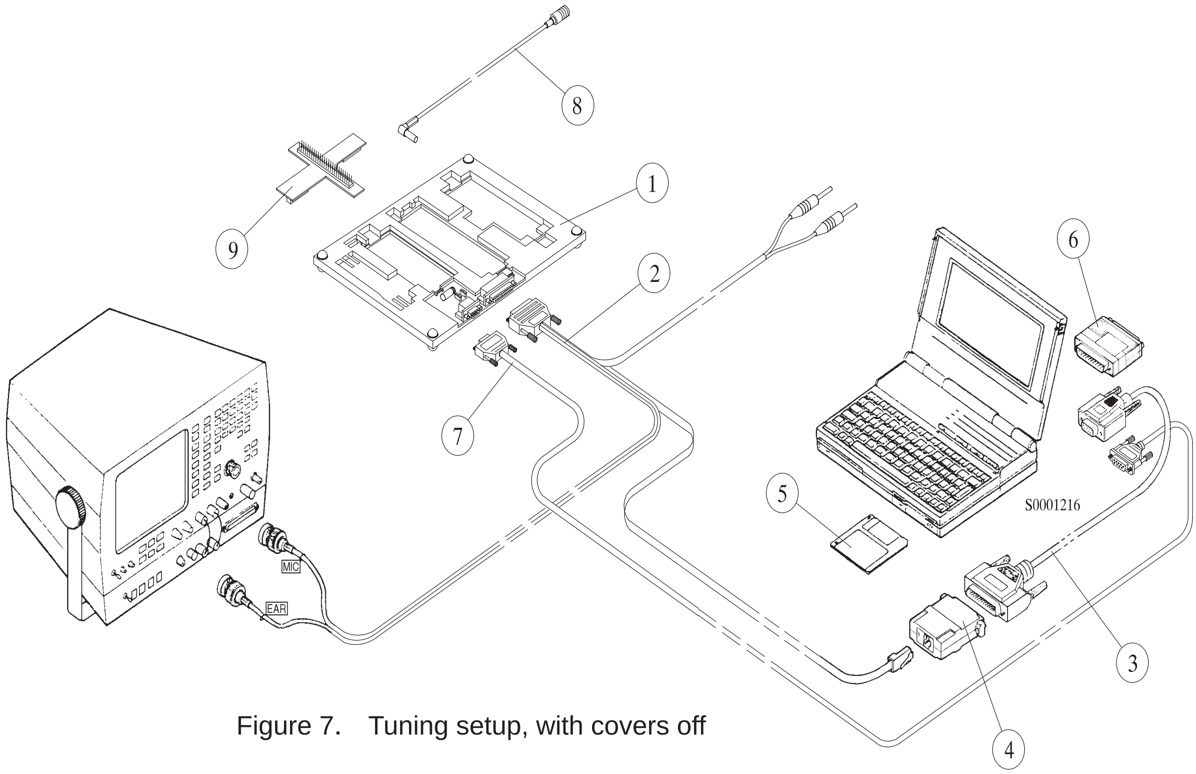


Figure 7.   Tuning setup, with covers off

1. MJS–1 MODULE JIG *
2. SCH–7 SERVICE CABLE *
3. RS232 9–25 PIN ADAPTER
4. DAU–2/2T
5. SERVICE SOFTWARE 3”DISK
6. PKD–1 DONGLE
7. SCR–3 SERIAL CABLE *
8. RF TEST CABLE (7100424) *
9. RBM–1 BOARD TO BOARD MEASUREMENT ADAPTER *

– HINGE FLEX (NOT SHOWN) *
– RBM–2 HINGE FLEX MEASUREMENT ADAPTER (NOT SHOWN) *

* INCLUDED IN MODULE JIG KIT MJS–1K

Tuning Procedure for GSM units

Carry out this procedure in the order as shown.

1. RSSI Reference Signal Level Storage

Reference value for the received signal strength meter are program tuned.

RSSI reference signal level programming:

- Start the service software and go to ”Main” menu.
- Select ”Phone mode” and select local mode with <Enter> key.
- Select ”Testing and Adjustments” menu and press <Enter>.
- Select ”Adjustments” menu and press <Enter>.
- Connect RF generator to antenna connector at 947.06771 MHz.
- Adjust signal generator level to –80 dBm + cable attenuation.
- Select ”RSSI Calibration” and press <Enter>.
- Adjust signal generator level to –50 dBm + cable attenuation. (see note below)
- Press <Enter>.
- DAC values should be in first row (0 dB) 450 – 700 and last row (57 dB) 750 – 1000
- Press <Esc> key.
- Store the value to the EEPROM with <Y> key.

2. AFC Diagram Storage

This tuning is used to calibrate the automatic frequency control range.

AFC tuning:

- Set RF generator frequency 947.06771 MHz at level –45 dBm.
- Select adjustments menu option ”AFC Diagram” and press <Enter>
- Check that ” Cont mode channel” is 60
- The measurement result should be;
  - Low over –22 kHz (< –8 kHz)
  - Middle ±1.5 kHz
  - High below +22 kHz (> 8 kHz)
- Press <Esc> key and store with <Y> key.

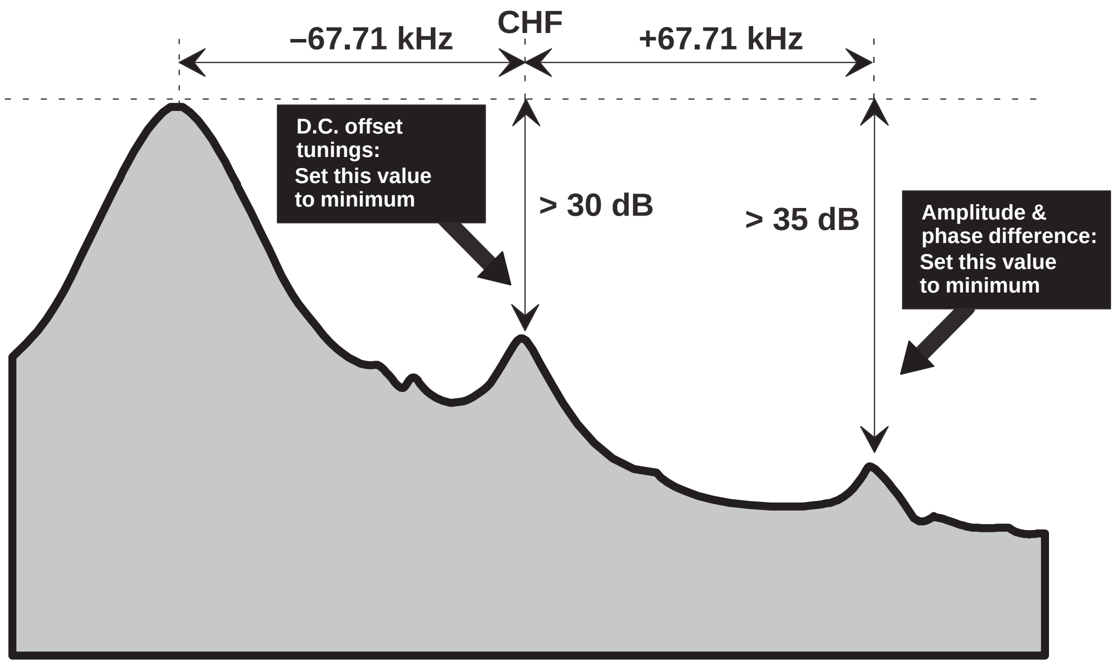
***Note**: Always take the target tuning value from the actual monitor screen as the value can vary according to which CMT software version is used.*

3. I/Q Modulator Amplitude Balance and Phase Shift Tuning

The purpose of this tunig operation is to adjust the I/Q modulator d.c. offsets and the I/Q modulator amplitude balance and phase shift.

I/Q modulator d.c. offsets, amplitude balance and phase shift tuning:

– Connect spectrum analyzer (with attenuator if needed) to external RF connector.
– Select adjustment menu option ”TX I/Q Tuning” and press <Enter>.
– Check that TX power level is level 10, Cont. mode channel is 60 and TX data type is 1.
– Adjust spectrum analyzer centre frequency to 902 MHz, Span 200 kHz, Res BW 10 kHz, Video BW 1 kHz and Sweep time 0.5 s.



– Select option ”TX I d.c. offset” and press <Enter>.
– Adjust the level of centre frequency (CHF signal) to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.
– Select option ”TX Q d.c. offset” and press <Enter>.
– Adjust the level of signal CHF to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.

– Select option ”TX I and Q d.c. offset” and press <Enter>.
– Adjust the level of signal CHF to minimum by varying D/A converter value with <+> and <–> keys.
– The amplitude difference between CHF–67.7 kHz and CHF should be >30 dB.
– When value is OK press <Esc>.
– Select option ”Tune Amplitude Difference” and press <Enter>.
– Adjust the level of signal CHF+67.7 kHz (902.06771 MHz) to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.
– Select option ”Tune Phase Difference” and press <Enter>.
– Adjust the level of signal CHF+67.7 kHz to minimum by varying D/A converter value with <+> and <–> keys.
– The amplitude difference between CHF+67.7 kHz and CHF–67 kHz should be >35 dB.
– When value is OK press <Esc>.
– Press <Esc> key and store new values with <Y> key.

4. Tuning of Transmitter Power Levels

This adjustment loads the power levels of the phone transmitter into the EEPROM. When doing this, a pulse power meter or spectrum analyzer must be used.

Note: *The cable loss of HCR–1 is about 1.0 dB.*

Power levels programming:

– Set power supply voltage to 7.2 V.
– Connect pulse power meter or spectrum analyzer to external RF connector.
– Check that channel 60.
– Select adjustments menu option ”TX Power Tuning” and press <Enter>.
– Press <Y>.
– Adjust the power level (levels Base, 5, 13 and 15) with <+> and <–> keys and change levels with <Up> and <Down> keys.

Power level	**Tuning P_{OUT}/dBm (VB=7.2 V, CH60)**
Base	0 *tune first !*
5	33 *tune !*
6	31
7	29
8	27
9	25
10	23
11	21
12	19
13	17 *tune !*
14	15
15	13 *tune !*

– Press <F3> to calculate all other levels.
– Once all TX levels are OK, press <Esc> and store readings in phone EEPROM with pressing <Y>.

5. Charge Voltage Adjustment

A reference value for charge voltage is set by using an accurate 6.0 V supply.

Calibration of the charge voltage:

– Apply +6 V to modular power connector, SCF–6.
– Select adjustments menu option ”Charge Voltage Adjustment”.
– Program reads 6 V, A/D reading fed to phone VCHAR line.
– Store charge voltage value to phone EEPROM by pressing <Y>

6. Battery Voltage Adjustment

A reference value for battery are calibrated by using an accurate 6 V supply.

Calibration of the A/D converter channels:

– Apply +6 V to carkit dummy test battery, BTD–1C
– Select adjustments menu option ”Battery Voltage Adjustment”.
– Program reads 6 V, A/D reading fed to phone VBATT line.
– Store correct value to phone EEPROM by pressing <Y>

Tuning Procedure for PCN units

Carry out this procedure in the order as shown.

1. RSSI Reference Signal Level Storage

Reference value for the received signal strength meter are program tuned.

RSSI reference signal level programming:

- Start the service software and go to ”Main” menu.
- Select ”Phone mode” and select local mode with <Enter> key.
- Select ”Testing and Adjustments” menu and press <Enter>.
- Select ”Adjustments” menu and press <Enter>.
- Connect RF generator to antenna connector at 1842.8677 MHz (Channel 700).
- Adjust signal generator level to –75 dBm + cable attenuation (see note below)
- Select ”RSSI Calibration” and press <Enter>.
- Adjust signal generator level to –45 dBm + cable attenuation.
- Press <Enter>.
- DAC values should be in first row (0 dB) 450 – 700 and last row (57 dB) 750 – 1000.
- Press <Esc> key.
- Store the value to the EEPROM with <Y> key.

***Note**: Always take the target tuning value from the actual monitor screen as the value can vary according to which CMT software version is used.*

2. AFC Diagram Storage

This tuning is used to calibrate the automatic frequency control range.

AFC tuning:

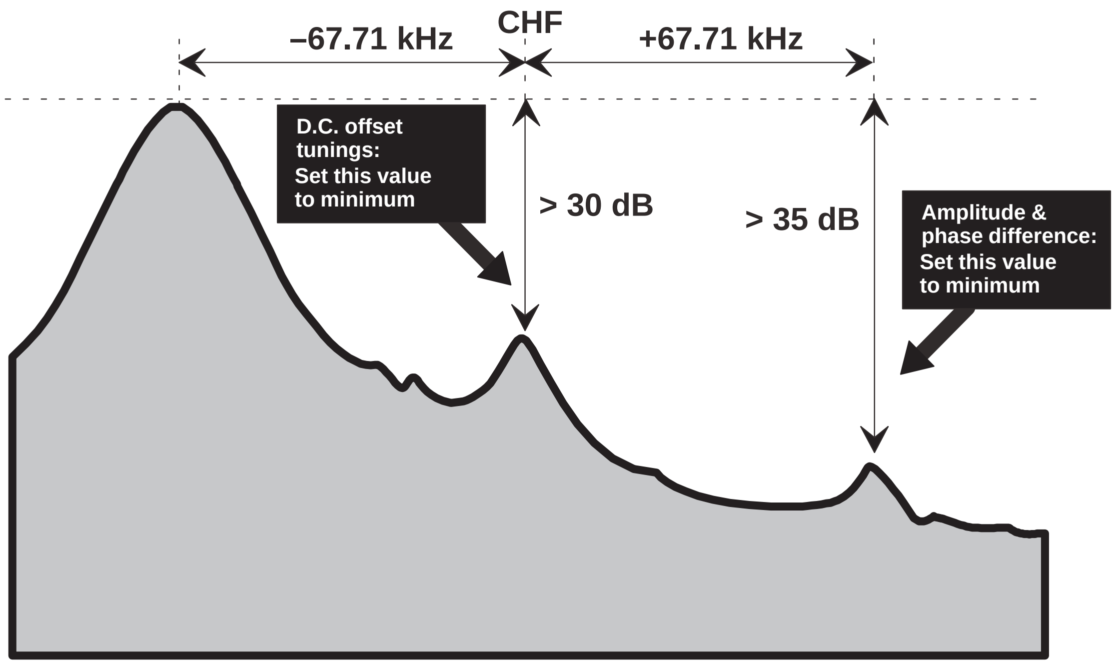
- Set RF generator frequency 1842.8677 MHz at level –45 dBm + RF cable attenuation.
- Check that ” Cont mode channel” is 700
- Select adjustments menu option ”AFC Diagram” and press <Enter>
- The measurement result should be;
  - Low between –30 kHz and –10 kHz, typically –20 kHz
  - Middle ±3.0 kHz
  - High between 10 kHz and 30 kHz, typically +20 kHz
- Press <Esc> key and store with <Y> key.

3. I/Q Modulator Amplitude Balance and Phase Shift Tuning

The purpose of this tuning operation is to adjust the I/Q modulator d.c. offsets and the I/Q modulator amplitude balance and phase shift.

I/Q modulator d.c. offsets, amplitude balance and phase shift tuning:

– Connect spectrum analyzer (with attenuator if needed) to phone antenna connector.
– Select adjustment menu option ”TX I/Q Tuning” and press <Enter>.
– Check that TX power level is level 5, channel is 700 and TX data type is 1.
– Adjust spectrum analyzer centre frequency to 1747,8 MHz, Span 200 kHz, Res BW 10 kHz, Video BW 1 kHz and Sweep time 0.5 s.



– Select option ”TX I d.c. offset” and press <Enter>.
– Adjust the level of centre frequency (CHF signal) to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.
– Select option ”TX Q d.c. offset” and press <Enter>.
– Adjust the level of signal CHF to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.

– Select option ”TX I and Q d.c. offset” and press <Enter>.
– Adjust the level of signal CHF to minimum by varying D/A converter value with <+> and <–> keys.
– The amplitude difference between CHF–67.7 kHz and CHF should be >30 dB.
– When value is OK press <Esc>.
– Select option ”Tune Amplitude Difference” and press <Enter>.
– Adjust the level of signal CHF+67.7 kHz to minimum by varying D/A converter value with <+> and <–> keys.
– When value is OK press <Esc>.
– Select option ”Tune Phase Difference” and press <Enter>.
– Adjust the level of signal CHF+67.7 kHz to minimum by varying D/A converter value with <+> and <–> keys.
– The amplitude difference between CHF+67.7 kHz and CHF–67 kHz should be >35 dB.
– When value is OK press <Esc>.
– Press <Esc> key and store new values with <Y> key.

4. Tuning of Transmitter Power Levels

This adjustment loads the power levels of the phone transmitter into the EEPROM. When doing this, a pulse power meter or spectrum analyzer must be used.

Note: *The cable loss of HCR–1 is about 2.4 dB*

Power levels programming:

– Set power supply voltage to 7.2 V.
– Connect pulse power meter or spectrum analyzer to antenna connector.
– Check that channel is 700.
– Select adjustments menu option ”TX Power Tuning” and press <Enter>.
– Press <Y>.
– Adjust the power level (levels Base, 0, 8 and 10) with <+> and <–> keys and change levels with <Up> and <Down> keys.

Power level	**Tuning P_{OUT}/dBm (VB=7.2 V, CH700)**
Base	0 *tune first !*
10	10
8	14
0	30

– Press <F3> to calculate all other levels.
– Once all TX levels are OK, press <Esc> and store readings in phone EEPROM with pressing <Y>.

5. Charge Voltage Adjustment

A reference value for charge voltage is set by using an accurate 6.0 V supply.

Calibration of the charge voltage:

– Apply +6 V to VCHAR line.
– Select adjustments menu option ”Charge Voltage Adjustment”.
– Program reads 6 V, A/D reading fed to phone VCHAR line.
– Store charge voltage value to phone EEPROM by pressing <Y>

6. Battery Voltage Adjustment

A reference value for battery are calibrated by using an accurate 6 V supply.

Calibration of the A/D converter channels:

– Apply +6 V to dummy battery.
– Select adjustments menu option ”Battery Voltage Adjustment”.
– Program reads 6 V, A/D reading fed to phone VBAT line.
– Store correct value to phone EEPROM by pressing <Y>

Chapter 8

Faultfinding/Disassembly

CONTENTS –Faultfinding

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Figures

General

The purpose of this document is to provide methods of finding component malfunctions in the PDA module of the Communicator.

Note:–Due to the large integration scale used it is not always possible to pinpoint the faulty component. However the flow diagrams introduced here should act as a useful guide for these purposes.

Required servicing equipment:

– PC for the service software

– power supply

– RS cable

– digital multimeter

– oscilloscope

– frequency counter (optional)

Disassembly Procedure

LCD / UI Module Disassembly (see fig.1)

1. Remove 4 stick–on screw caps (A) and 4 Torx screws (B).
2. Gently remove the module sub–assy by pushing the keypad down.

   Note: *The right lower screw tower is the most difficult one to release.*
3. Disconnect flexi connectors (D) then (C) by releasing connector clips. Connector C will open by lifting the clip up.
4. Unplug the coaxial antenna wire. (E).
5. Remove EMC flex (not shown) from the reverse side of the UI module card and then remove the module assembly. (F).
6. Remove PDA LCD module assy. (H)
7. Unclip screen frame (G) from the LCD module.

   Note: *LCD module is attached to the frame by double sided tape.*
8. Re–assemble in reverse order ensuring the following:
   - correct orientation of PCB in frame, i.e. connector D should be in line with the scroll keymat.
   - Coaxial antenna cable (E) does not go under the UI module or it will disable the function keys.

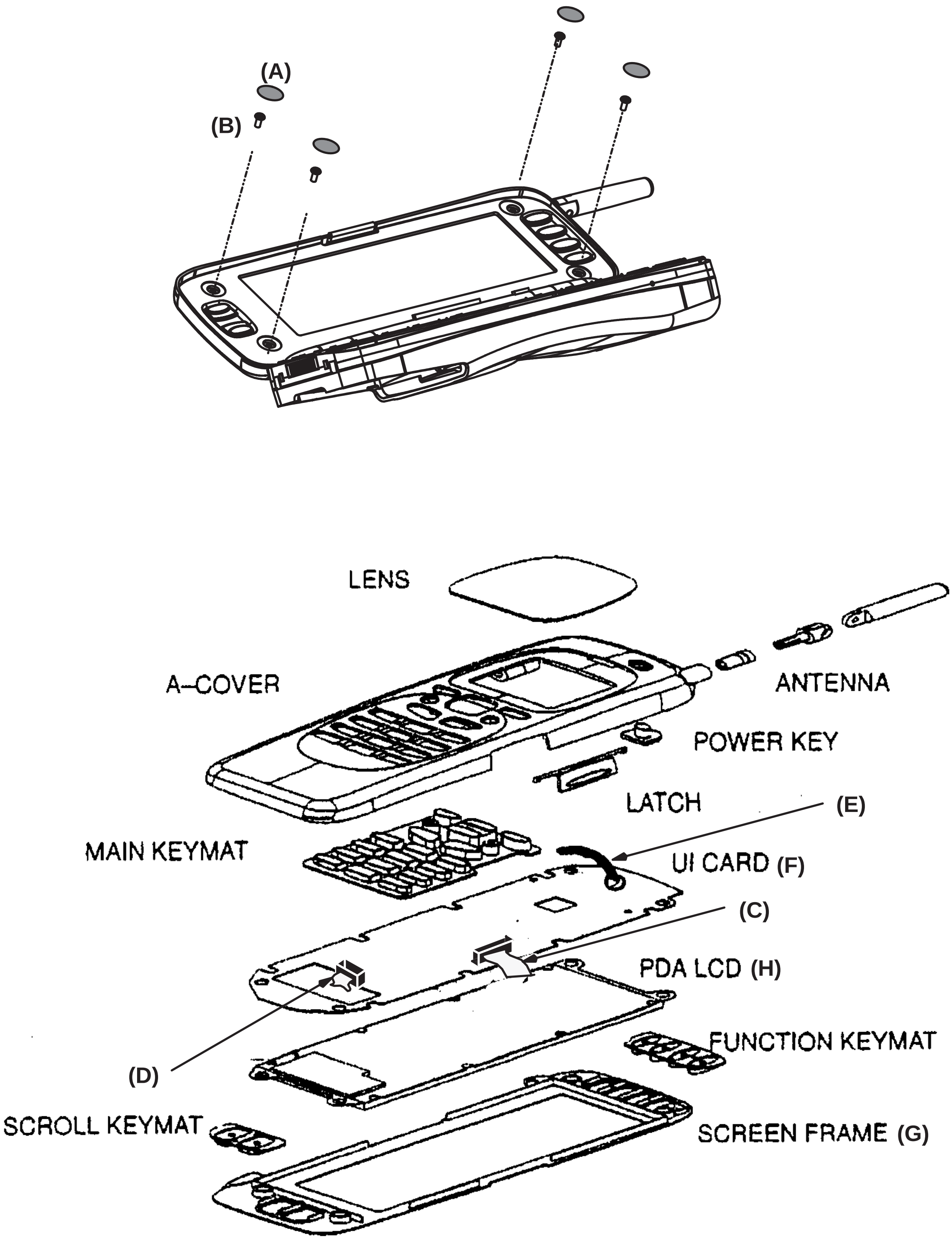


Figure 1. LCD / UI Module disassembly

System Module Disassembly (see fig.2)

1. Remove Battery. (A)
2. Remove 2 Torx screws. (B)
3. Gently lift off C cover (C) starting from the battery hole.

   Note: *be aware that the speaker gasket on the SIM–flex might stick to the C cover buzzer gasket.*
4. Remove 7 torx screws, (D) do not undo screws marked with an S on the diagram yet.
5. Remove coaxial antenna cable. (E)
6. Remove EMC flex (not shown) from the top of the shield.
7. Lift out the sub–assy.
8. Remove PDA module card (I) from the chassis by lifting it in the middle.
9. Remove the handsfree speaker from the chassis.
10. Open the SIM–flex connector on the CMT module and unplug the SIM–flex from the chassis. (F)
11. Remove 3 short Torx screws (S), open the shields and remove the CMT module.
12. Re–assemble in reverse order and observe the following points:
    - Ensure the shield snaps into position properly.
    - Position the handsfree speaker gasket so that the sound gap in the chassis is open and the speaker wires are not trapped between the PDA module and chassis.
    - Check that the handsfree microphone wires go through the slot in the chassis and do not get trapped between the chassis and PDA module.
    - Position the EMC flex with guide lines on the shield.
    - When re–assembling the sub–assy and cover, locate the system connector end of the assy first.
    - Ensure the handsfree microphone dust washer inside the cover remains in place.
    - Position the coaxial antenna cable so that it goes around the screw tower. The black mark on the cable is the correct fixing point for the cover.

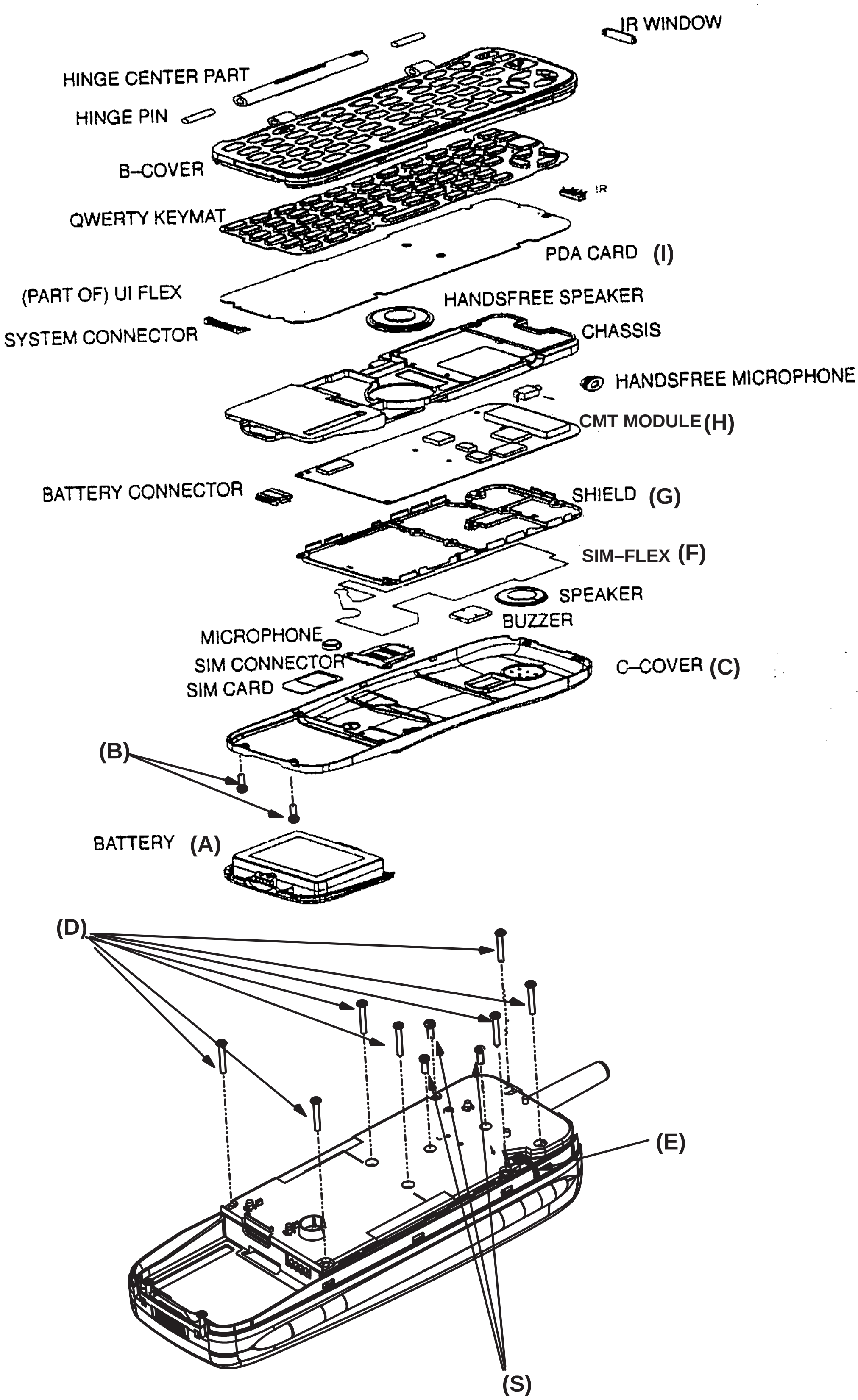


Figure 2. System Module disassembly

PDA Faultfinding

Introduction

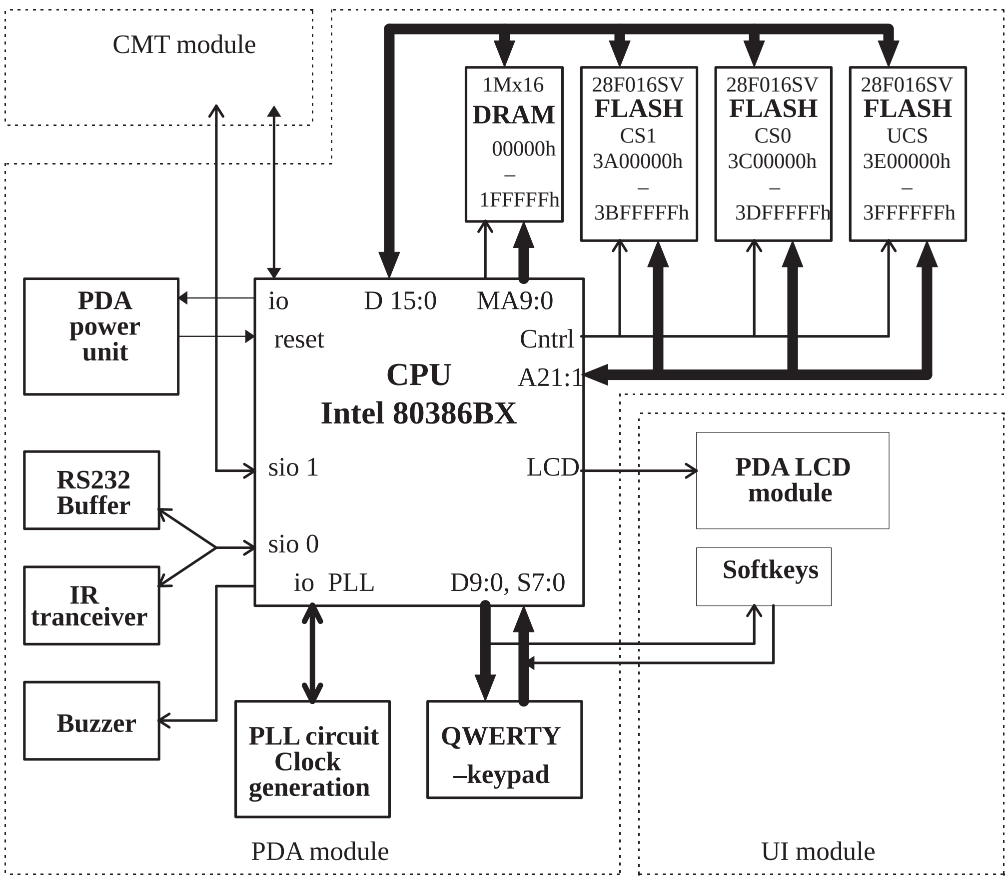
The purpose of this document is to provide methods to find the component that is malfunctioning in the PDA module of the Communicator. Due to the large integration scale used in the Communicator, it is always not possible to point the faulty component for sure. However the flow diagram introduced here is made to fulfill the aim as well as it is possible.

Required Servicing Equipment:

– PC for the PCLocals
– power supply
– RS cable
– digital multimeter
– oscilloscope
– frequency counter (optional)

Block Diagram

The block diagram of the Communicator PDA is described in the picture below:



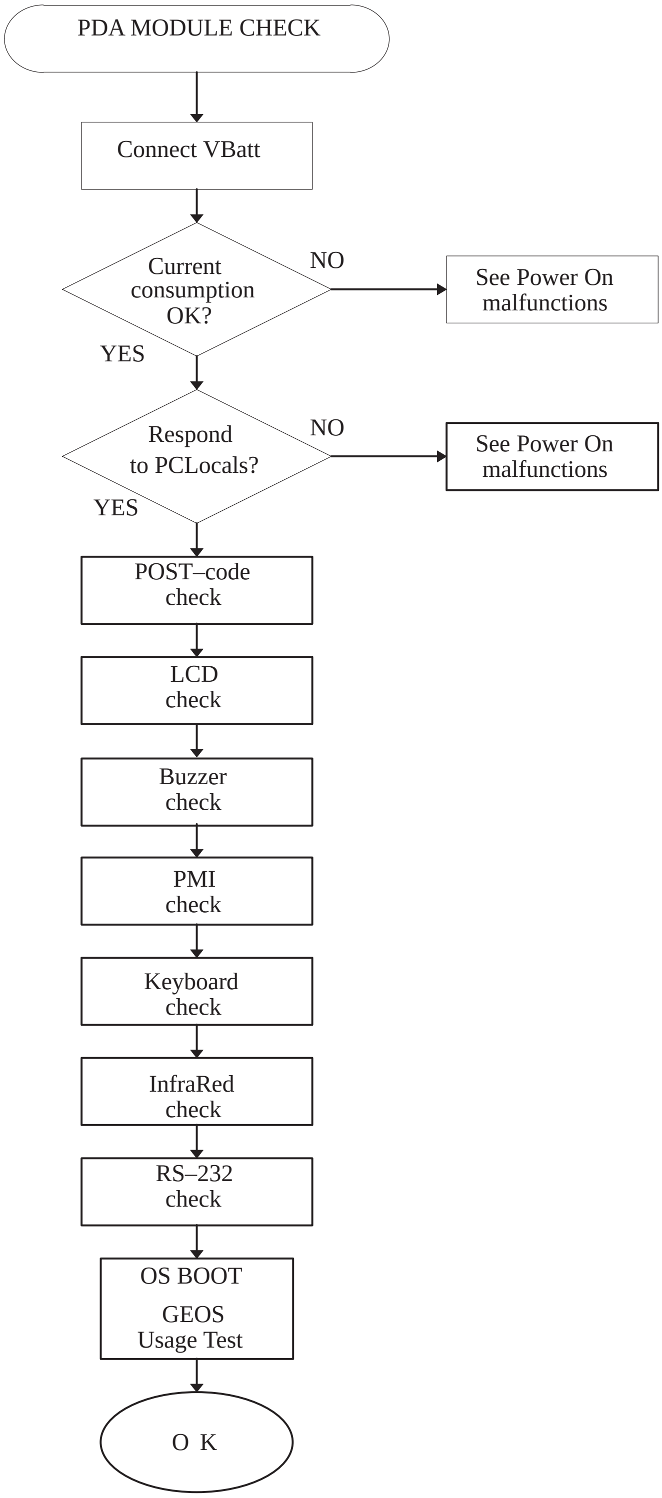
PDA Components

The following components of the Communicator PDA have an dramatic effect to the functionality of the module, a fault in any of these may cause the module to appear totally 'dead':
– PDA power unit
– CPU
– PLL clock generation circuit
– UCS Flash chip

If the device has some functionality, then the following components, along with the ones above, can be tested:
– DRAM chip
– CS1 and CS0 Flash chips
– RS buffer
– buzzer
– IR tranceiver
– keyboard
– LCD module

PDA Troubleshooting Diagram

The highest level of PDA troubleshooting is shown in the following flow chart. All diagrams assume that the unit has been checked for short circuits and loose pins.



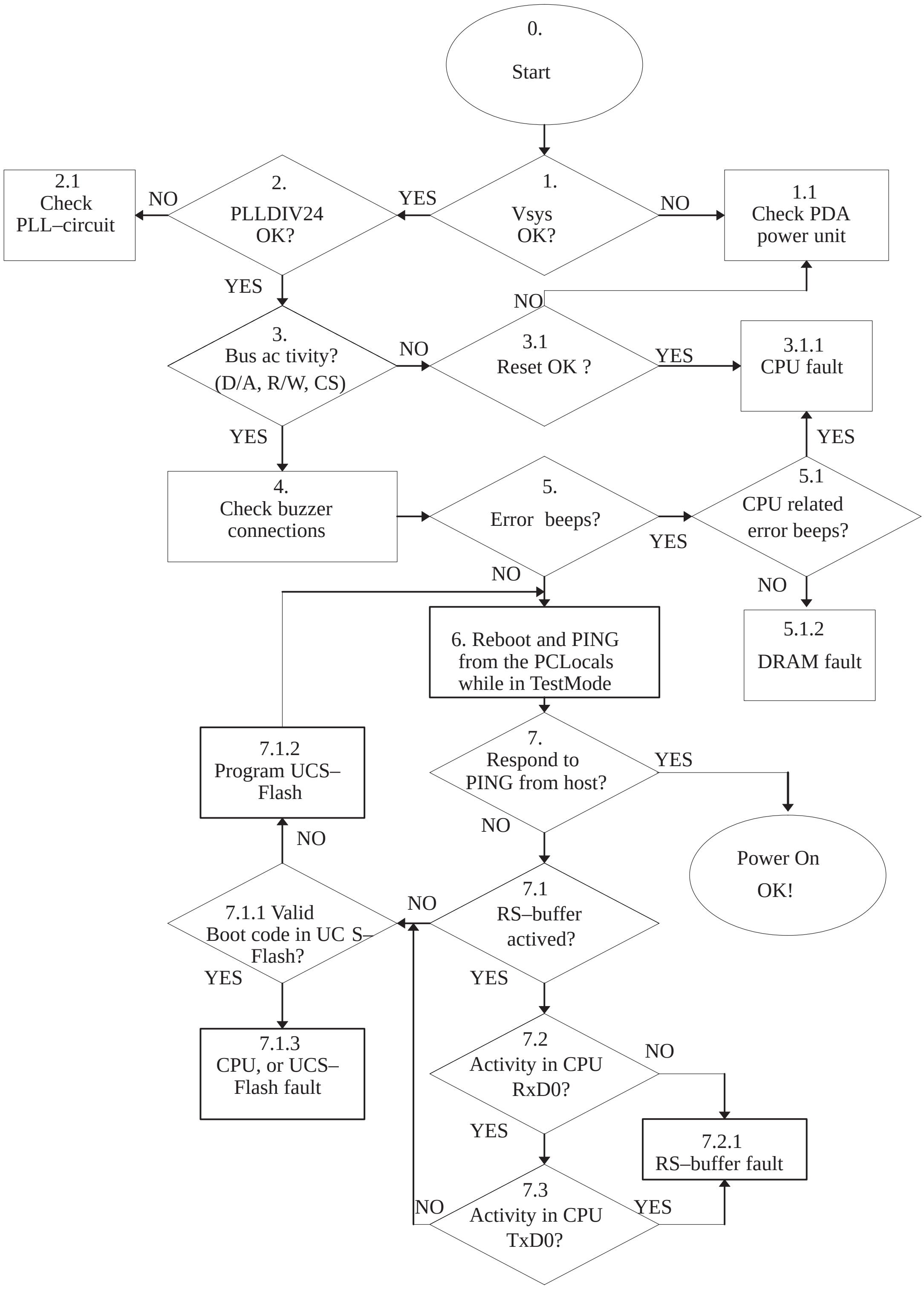
The module check begins with connecting the supply voltage to the PDA. If the current consumption differs a great deal from the normal limits, proceed to the Power–On check.

If current consumption is OK, the service software should connect to the PDA. If the target PDA does not respond to the pings from the host, check the Power–On procedure.

When the PDA responds further tests may be carried out; the execution order is not significant and it may be changed.

After all the functional tests are working, the device under test should be re–booted, and the normal usability of the GEOS, along with the CMT module should be checked before the PDA can be considered to be fully functional.

1 Troubleshooting Diagram of the Power–On Malfunction



1.1 Vsys OK?

Start the Power–On check by connecting the power supply to the target. The power supply voltage limits are: 5.8V (min.) – 7.2V (nom.) – 8.5V (max), The current consumption in a working PDA is typically about120mA.

If the Vsys is out of the limits (2.97V..3.66V) or the current consumption differs from the normal, then check the PDA power unit.

1.1.1 Check PDA Power Unit

The following picture illustrates the troubleshooting diagram that can be used with the PDA power unit malfunctions. As a rough check it is good to glance through the power section of PDA module and check that there are no short circuits by alien particles and that no component has ’burning’ signs, especially tantalum capacitors. If yes, the fault is most probably cured by replacing that component. In such a case it is recommended that the complete power unit check is done after replacing the faulty component.

If power unit check is not solving the problem there is a possibility that battery line or some regulator output has a short circuit somewhere. Vsys is distributed all over the board and it may be difficult to find possible short circuit cause. There are test strips going to the edge of PCB in middle layers. The strips are cut when the module is cut from the panel in production. If the device is used in high moisture environment it is possible that those copper strip ends corrode and form some ohmic short circuit to neighbouring strips. Use of glass fibre brush to test strip ’necks’ on the edge of PCB is recommended. Current supplying capabilities of different regulators are: Vsys:500mA, VCC5:50mA, LCDVEE:5mA. Each current is for the specific regulator output voltage. VCC5 is linear regulator, VSYS and LCDVEE are made by switch mode regulators.

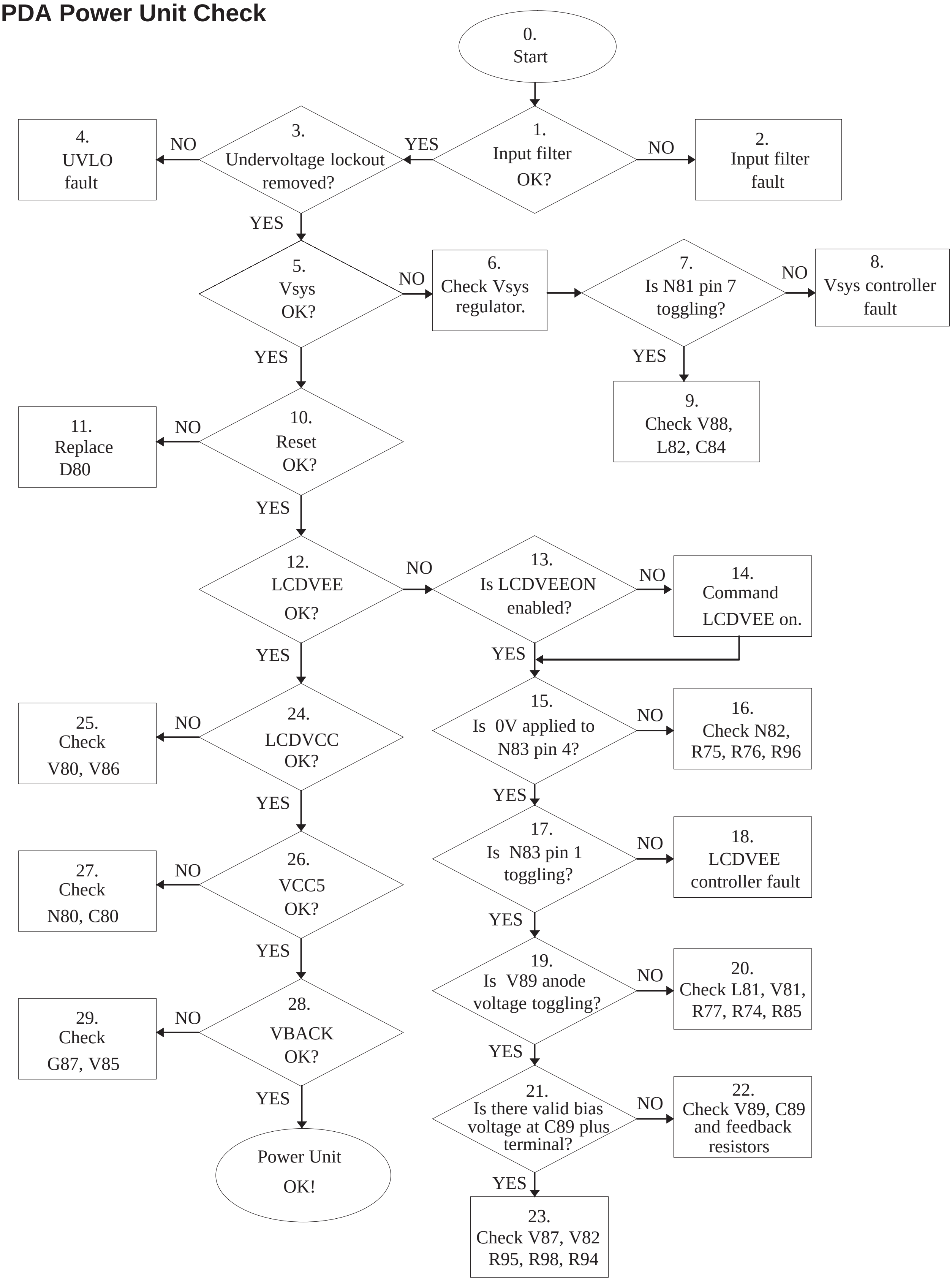
1.1.1.1. Input filter OK?

Between board–to–board connector battery line and regulators there is LC–filter to reduce interference conducting through battery line from CMT to PDA module and visa versa. Overcurrent and overvoltage may damage filter components. If battery voltage is not seen in equal value at positive terminal of C83 and at board–to–board connector battery line then check that L80 is not open circuited. If not check that C81 and C83 are not short circuited to a finite resistance (<100 ohm) and there is no visible damage in capacitors. If fault is still not found check also bypass capacitors C93, C94, C96, C87 and C97.

1.1.1.2 Input filter fault

Replace faulty component. If fault is not focused try to change tantalum capacitors first. If that is not helping there is a possibility that one of the IC’s N80, N81, N82 or N83 has internal short circuit.

PDA Power Unit Check



1.1.1.3 Undervoltage lockout removed?

This UVLO is made as hardware limit to shut down Vsys if battery voltage drops below 5.0V. **When the N82 comparator controlling N81 has worked the shutdown of Vsys is cancelled only after battery voltage rises over 6.0V!** It is possible to test PDA module at voltages between 5.0V and 6.0V but wakeup of Vsys requires voltage higher than 6.0V. This hysteresis is put to design to prevent oscillation at low battery voltages after battery cutoff limit is reached and battery voltage rises after its load is removed.

If battery voltage is higher than 6.0V, battery voltage (nearly) should be seen at regulator N81 pin 1. If not go to 1.1.1.4.

1.1.1.4 UVLO fault

First check that 4.1V can be measured from reference V84 cathode. If not replace V84 and check R88. Next check that voltage between R87 and R89 is higher than voltage across V84. This voltage should be reduced to V84 voltage level if battery voltage is reduces to 5.0V. If not check R87, R89 and R65.

If above mentioned is OK check R80. If OK replace N82.

1.1.1.5 Vsys OK?

Measure Vsys voltage for example from C84 positive terminal. It should be between 3.135V and 3.465V. If not go to 1.1.1.6.

1.1.1.6 Check Vsys regulator

First check that battery voltage is seen at N81 pins 3 and 8. If pin 3 is low regulator does not exit from ’soft start’ state.

1.1.1.7 Is N81 pin 7 toggling?

If measured with oscilloscope there should be seen voltage level toggling between 0V and VBatt at frequency of about 200kHz. If not go to 1.1.1.8. Otherwise go to 1.1.1.9. If the regulator has dropped to a shutdown state the pulse frequency is lower and pulses appear at irregular time intervals.

1.1.1.8 Vsys controller fault

Replace N81.

1.1.1.9 Check V88, L82, C84

If the controller N81 tries to alternate pin 7 level, even at reduced voltage magnitude the fault is very likely found from V88, L82 or C84. If the problem is still unsolved check that Vsys current consumption is less than 500mA. Reasonable value is about 200mA when CPU is fully on. If not there must be a short circuit in Vsys line.

1.1.1.10 Reset OK?

The PWRGOOD signal should go from low to high after minimum time of 140ms when Vsys has risen to a valid level. Time between battery connection and valid voltage at Vsys line should be in the order of 1.5ms. If PWRGOOD signal rises too fast, or the signal levels are illegal, then go to 1.1.1.11.

1.1.1.11 Replace D80

If this is not helping PWRGOOD line is pulled up or down somewhere or there is a CPU fault.

1.1.1.12 LCDVEE OK?

In boot sequence LCD is on. If voltage other than 20V – 24V near room temperature is seen at LCDVEE terminal then go to 1.1.1.13.

1.1.1.13 Is LCDVEEON enabled?

There is LCD bias voltage shutdown feature in PDA normal use after set inactivity time period. Check that LCDVEEON line is in logic high state (3.0V – 3.4V). If not go to 3.1.1.14. Otherwise go to 1.1.1.15.

1.1.1.14 Command LCDVEE on

Use PC Locals to command LCDVEE permanently on. Select 'I/O–Space Functions'/'Target Signal Control' to toggle LCDVEE. This menu can also be used to control LCDVCC, flash program voltage (VCC5) and LCDPWM. When LCD module is not connected verify also LCDVEE off state by toggling the control by PCLocals.

1.1.1.15 Is 0V applied to N83 pin 4?

Check that voltage between 0V and 0.3V is seen at N83 controller pin 4. This signal enables the controller. If not go to 1.1.1.16. When LCD module is not connected verify also LCDVEE off state by toggling the control by PCLocals. In LCDVEE off state N83 pin 4 must see battery voltage.

1.1.1.16 Check N82, R75, R76, R96

First check that resistors R75, R76 and R96 are OK. Check that voltage at comparator N82 pin 3 is in the range of 1.55V – 1.75V. If not check reference V84. In cathode of V84 voltage of 4.1V should be seen. If OK replace N82. After that if still problems verify that comparator N82 pin 2 has higher voltage than pin 3. If yes and N82 pin 1 is not low (0V – 0.3V) then change N83.

1.1.1.17 Is N83 pin 1 toggling?

There should be seen about 300kHz voltage toggling between 0V and VBatt. In oscilloscope there should be seen about 20 pulse sequences at irregular pulse group periods. If not go to 1.1.1.18. Otherwise if there are pulses coming to N83 pin 1 in continuous train the regulator is ’saturated’. Check that valid LCD voltage is seen at C89 positive terminal. Measure LCDVEE current with UI module connected. If current is higher than 4mA big LCD in UI module is probably corrupted.

1.1.1.18 LCDVEE controller fault

Replace N83.

1.1.1.19 Is V89 anode voltage toggling?

There should be seen irregular shaped voltage bursts at peak magnitude between 0V and valid LCD voltage (little higher). Voltage bursts decrease in magnitude during their period. The bursts appear at irregular time intervals. If not go to 1.1.1.20.

1.1.1.20 Check L81, V81, R77, R74, R85

Most probably V81 is broken. Check and replace. If not helping check L81 and R74, R85. These resistors provide current feedback information to the controller. There should be seen increasing voltage spikes at peak magnitude of a little less than 300mV. If yes L81, V81, R74 and R85 are OK. Then check and replace V89.

1.1.1.21 Is there valid bias voltage at C89 plus terminal?

Measure DC voltage over C89. It should be within 20V – 24V at room temperature. Measure also peak–to–peak AC voltage from 100ms sample. It should be less than 100mV. If not go to 1.1.1.22. If yes go to 1.1.1.23.

1.1.1.22 Check V89, C89 and feedback resistors

First measure voltage from N83 pin 3. It should be exactly 1.5V. If yes replace C89. Also check C95 and V89. If not check resistance and replace if needed for resistors: R84, R82, R78, R93 and R97. Also check C79.

1.1.1.23 Check V87, V82, R95, R98, R94

The fault is that the regulator works correctly but the switch between the regulator and LCD module is broken. This switch is needed to totally cut voltage from LCDVEE line. First measure collector voltage of V87. It should be near 0V. If not check and replace V87, R95 and C98. If yes replace V82. Also check R94 and R98.

1.1.1.24 LCDVCC OK?

Command LCDVCC on by PCLocals. Measure voltage from LCDVCC line. If the voltage differs from Vsys value go to 1.1.1.25. When LCD module is not connected verify also LCDVCC off state by toggling the control by PCLocals.

1.1.1.25 Check V80, V86

Transistor V80 gate is pulled down by transistor V86 to enable LCDVCC. Identify and replace the faulty transistor. If not helping then check also R81, R72 and C91.

1.1.1.26 VCC5 OK?

Command VCC5 on by PCLocals. Measure voltage from VCC5 line. If the voltage is other than 5.00V ±50mV go to 1.1.1.27. The delay between regulator enable and valid voltage at output should be less than 0.1ms.

1.1.1.27 Check N80, C80

Check that CPU enable signal comes to regulator pin 3. If yes try to disconnect VCC5 load by bending up N80 pin 5 and attaching output capacitor to the pin. If regulator works after that there is failed ohmic connection in VCC5 line or in FLASH memories. Otherwise check and replace N80, C80.

1.1.1.28 VBACK OK?

Measure backup battery voltage from battery terminals. If that is less than 2.8V backup battery is about to be empty in near future (80% used). Then it is reasonable to change the battery in order to save customer from inconvenience in near future. In order to do complete test disconnect main battery from the module. If voltage in VBACK line is under 2.6V go to 1.1.1.29.

With PC Locals it is possible to check whether the VBACK voltage has been on illegal level before boot. This can be checked only once after each boot, and then after the VBACK is considered to be OK.

1.1.1.29 Check G87, V85

Check that voltage over G87 is 2.8V or higher. If not check that there is maximum 35mV drop over resistor R90. If the drop is higher, RTC circuitry in VBACK line take too much current. If the drop is OK check that VBACK line voltage drop in diode V85 is less than 150mV. If not replace V85.

1.2 PLLDIV24

If the Vsys and the current consumption is OK, check whether the PLL circuitry and the clock generation inside the CPU (D130) is working properly. The output of pin 110 of the CPU should be a square wave and the frequency in A5 stepping of the CPU 307kHz, in the A3 stepping of the CPU the frequency should be 614kHz. The shape and the frequency can be checked with a scope, the frequency can be measured more accurately with a frequency counter.

If the frequency is OK, then proceed to 1.3 otherwise check the PLL circuitry 1.2.1

1.2.1 Check PLL Circuitry

The crystal and circuitry around it can be checked by connecting oscilloscope XTALI signal. On that point a 32.6 – 32.8 kHz signal with 2.5 – 3.5V peak to peak AC amplitude should be found. The signal waveform can vary from almost square wave to sine wave. If this signal can not be detected and VCCRTC level is 2 – 3V then check crystal and circuitry (R140, R141, R146, R147, C155, C156) around it. It is also possible that the actual CPU chip is defective.

If the XTALI signal is OK but PLLDIV24 signal is not available, LPLLI components (R136, C151, C152) and IREFL (R138) must be checked V131, C147 and C149 are also crucial for PLL functionality. If all these seem to be OK, the actual CPU chip is probably defective.

1.3 Bus Activity in Address/Data, Read/Write and Chip Selects?

If the PLL is functional, then the CPU system clock should be running and should try to fetch code from the Flash that is controlled by the UCSX.

Analyzing the code fetching cycles is beyond the scope of this document, and is not needed during normal troubleshooting. The main idea of this is just to check the signal levels, and to see that there is something happening, i.e. the CPU is not totally ’dead’.

If there is some bus activity in all data lines and the signal levels are adequate, the data bus can be considered to be functional. If there is some bus activity in the lower address lines and the signal levels are adequate, the address bus can be considered to be functional. The CPU should also try to read data from and to the memories also the UCSX line should toggle within normal voltage limits. If there are illegal signal levels, the faulty component can be isolated by disconnecting each component in the signal line one by one.

The cycles vary according to the code in the D163 Flash and therefore there is not necessarily no activity in MEMWX and the CS1/CS0 lines.

If there is no activity at all, then check PWRGOOD signal during powering the device up. If there is reasonable activity in the signals and the signal levels are OK, proceed to 1.4

1.3.1 Reset OK?

The PWRGOOD signal, coming from the PDA power unit, should go from low to high after 140ms when VBatt is connected. If this signal is not functioning as expected, then disconnect the signal either from the CPU (D130) or the Reset IC (D80), and isolate the problem to the power unit or to the CPU.

If this signal rises too fast, or the signal levels are illegal, then check the power unit. If the signal is OK, but there's no bus activity at all, then suspect a CPU fault, see 1.3.1.1

1.3.1.1 CPU Fault

If the PLL is running properly and the CPU gets the RESET signal from the power unit (PWRGOOD), but there is no bus activity at all, then it is likely that the CPU is not functioning properly.

If the PLL circuitry surrounding the CPU is OK, but the PLLDIV24 is not, then it is likely that the CPU is defective.

It is possible that PLLDIV24 is OK as well as RESET but no activity is detected on CPU address lines. Before you replace the CPU it is reasonable to check that circuitry around the HPLLI (R137, C153, C154) and IREFH (R139) is OK. It is hard to measure these signals so a visual check is usually all that can be done. If no defect can be found, suspect a defective CPU chip.

If the device beeps during POST CPU related error beeps, then it's likely that the CPU is defective.

1.4 Check Buzzer Connections

In the case of POST found error, the PDA can beep an error code. The list of the possibly error codes can be found in the appendix A. In order to hear the possible beeps, the connection from the CPU (D130) pin124 to the buzzer must be functional, i.e. the SIM flex should be connected to the CMT, and the PDA–CMT connection must carry a BUZZEROUT signal.

The beeps can be also seen using a scope connected to the CPU, pin 124, where the beeps generate a square wave. If the signal can be seen but no sound is heard, then check the circuitry R142–R148, V132–V135, C138, and the SIM flex etc.

1.5 Error Beeps

If there are some error beeps, then make the difference between CPU– and DRAM–related errors and proceed to the CPU/DRAM fault. If no beeps are generated then proceed to 1.6

1.5.1.2 DRAM Fault

If DRAM related error beeps can be heard, then check the resistors R180 – R195. If they are OK, then the fault can be either in the CPU (D130) or in the DRAM itself (D160). As the DRAM is easier to change, it is better to try that first.

1.6 Reboot and PING from the PC Locals while in Testmode.

Next try to establish a connection from the service software to the PDA. Activate the testmode pin of the PDA. Select a menu from the software that pings the target, and then reboot the PDA.

Pinging the target sends bytes (55h) to the PDA via the serial RXD, and waits for a response byte (AAh) from it via the TXD.

1.7 Respond to PING from the Target

If the target PDA respond to the host’s request, the Power–On procedure has succeeded and further tests can be carried out by proceeding to the uppermost level of the fault finding tree.

If no acknowledge is received, then proceed to 1.7.1

1.7.1 RS–Buffer Activated?

If the service software cannot receive the acknowledgement, then the fault can be in the CPU (D130), in the boot code that is located in the UCS Flash device (D163), or in the connection between the CPU and the host PC.

First check the connection:

During startup the CPU (D130) enables the RS–buffer MAX3222 (D180) by setting the RSENX (D180/pin1) low, RSSHDX (D180/pin20) high and the IRSHD (M180/pin6) high. The signals RSENX and the RSSHDX are toggled for the period of time that the CPU waits for a ping from the host, typically 3.5s. Check if this happens and whether the signal levels are OK.

If the signals are OK, then proceed to 1.7.2. If the CPU does not control the lines correctly, then proceed to 1.7.1.1

1.7.1.1 Valid Boot Code in UCS Flash?

If the boot code in the D163 is corrupted, then proceed to the 1 .1 If the Flash is programmed, or it is sure that it contains valid data, and the CPU doesn’t control the RS–buffer correctly, then proceed to 1.7.1.3

1.7.1.2 Program UCS Flash

If there’s no guarantee that the UCS Flash (D163) contains a valid boot code, re–programme it with the JTAG method, or change to a good one. After programming / replacing, return to 1.6

1.7.1.3 CPU, or UCS–Flash Fault

If the CPU (D130) doesn’t control the RS–buffer although there is a valid boot code in the UCS Flash (D163), then there is a fault either in the CPU, or in the Flash itself. In most cases the fault is likely to be the CPU, but it cannot be guaranteed unless the functionality of the UCS Flash is verified with another system.

1.7.2 Activity in CPU RxD0 ?

If the RS–buffer is activated and the IR–tranceiver TFDS3000 (M180) is put to active shutdown, then it’s worth checking if the RSRXD line (D130/pin114 –D180/pin10) is toggling, i.e. are the host’s pings received this far. If the line is toggling, and the signal levels are OK, then the CPU receives the ping bytes.

If the RSRXD line is not toggling, but the input of the buffer RXD (D180/pin9) is toggling, and the buffer control signals are OK, then proceed to 1.7.2.1. If the RSRXD signal is toggling (in the CPU pin), then the CPU should be transmitting acknowledgement bytes to the host. In the case proceed to 1.7.3

1.7.2.1 RS–Buffer Fault

In the case that the signals seem to stop to the buffer (D130), although the buffer control signals are set OK, then the buffer is likely to be defective.

1.7.3 Activity in CPU TxD0?

If the CPU receives the pings, then it should send acknowledgements through the RS–buffer to the service software. If the RSTXD line is not toggling, but the RSRXD is, then proceed to 1.7.1.1 If the RSTXD line is toggling but the TXD is not, then go to 1.7.2.1

2 Troubleshooting Diagram of the POST–Code

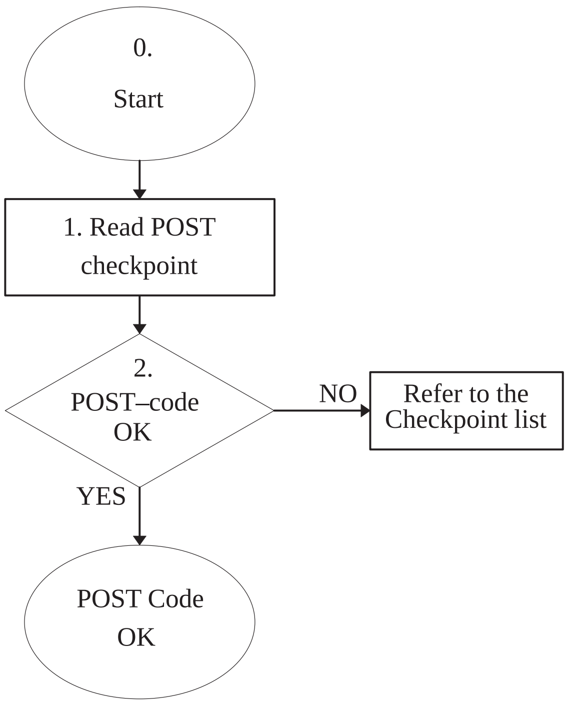
If the communications channel between the PDA and the service software can be established, the last checkpoint passed during POST can be retrieved from the PDA. The list of the POST–codes is in appendix B.

2 .1 Read POST Checkpoint

In order to read the POST checkpoint, choose the Get POST Checkpoint menu in the PC Locals.

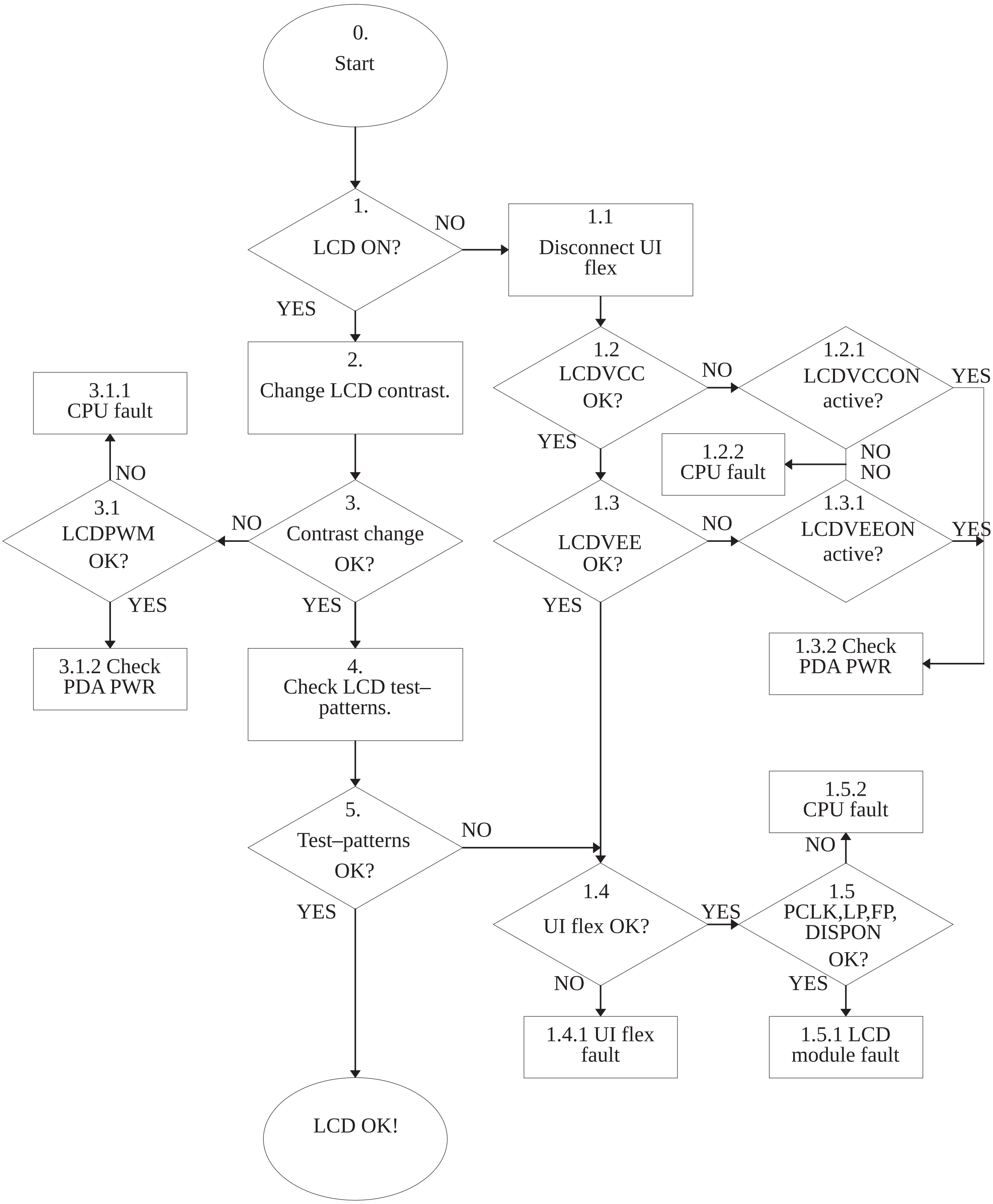
2 .2 POST–code OK?

If the checkpoint is right, i.e. equal to the one last in the list, the POST has completed successfully, and there are no bad errors in the internal parts of the CPU and none in the DRAM. If the checkpoint differs from the one that is expected, then refer to the checkpoint list. The possible errors can be divided mainly into two groups; CPU–, and DRAM–related errors.



3 Troubleshooting Diagram of the LCD Check

The following diagram is to differentiate between an LCD module or a PDA fault. An LCD module fault is beyond the scope of this document and requires that a replacement module be fitted.



3.1 LCD ON?

The first step is to check whether the LCD is on when in testmode. When the PDA boots, and if the testmode pin is active, the CPU controls the LCD on. If the LCD remains blank, then proceed to 3.1.1. If the LCD is set on, then more detailed tests can be carried out when proceeding to 3.2

3.1.1 Disconnect UI Flex

In order to isolate the problems in the LCD module, disconnect the UI flex from the PDA. Of course it can be easily tested if the problem disappears when connecting a working LCD module to the PDA.

If the problem can be isolated to the PDA module, then proceed to 3.1.2

3.1.2 LCDVCC OK

Check if the LCDVCC is within it’s legal limits 4.5V..4.8V. If not, then proceed to 3.1.2.1. If yes, then go to 3.1.3

3.1.2.1 LCDVCCON active

If the LCDVCCON is active (high) but the LCDVCC level is out of the limits then proceed to 3.1.3.2. If the CPU does not control the LCDVCCON active, then go to 3.1.2.2

3.1.2.2 CPU Fault

If the CPU does not control either the LCDVCCON or / and the LCDVEEON, and the signals are not forced low in the PDA power unit, then the CPU is defective.

3.1.3 LCDVEE OK?

Check if the LCDVEE is within it’s legal limits 19V..23V. If not, then proceed to 3.1.3.1. If yes, then go to 3.1.4

3.1.3.1 LCDVEEON Active?

If the LCDVEEON is active (high) but the LCDVEE level is out of the limits then proceed to 3.1.3.2 If the CPU does not control the LCDVCCON active, then go to 3.1.2.2

3.1.3.2 Check PDA Power Unit

If the CPU controls the LCDVCCON active, but the LCDVCC is out of the limits, check the PDA power unit. Check components V80, V86, R81, R72 and C91.

In a case that the CPU controls the LCDVEEON active, but the LCDVEE is out of the limits, check the PDA power unit. If voltage at positive terminal of C89 is not between 20V and 24V go to PDA power unit complete check to 3.1.1. Check V84, R75, R76 and R96. There must be 4.1V voltage difference over V84. If OK check that N83 pin 4 is in low

logic level voltage (0 – 0.3V). If not replace N82.
Otherwise check V87 and V82. Voltage at gate pin of V82 should be one third of the voltage seen at plus terminal of C89. Voltages at LCDVEE line and C89 plus terminal must be practically equal.

3.1.4 Check UI Flex

In a case that the LCDVCC and the LCDVEE are within their voltage limits, the fault is likely in the other controlling signals. But first it is good to check the UI flex. If the UI flex is OK, proceed to 3.1.5, otherwise go to 3.1.4.1

3.1.4.1 UI Flex Fault

Change the UI Flex.

3.1.5 Check PCLK, LP, FP, DISPON

If the CPU does control the PCLK, LP, FP and the DISPON in a reasonable manner, then proceed to 3.1.5.1 If one of the synchronizing signals (PCLK, LP, FP) remain still all the time, or if the DISPON is inactive (low), then go to 3.1.5.2

3.1.5.1 LCD Module Fault

If all the control signals are OK at the end of UI flex, then the possible fault is either in the LCD module or in the UI module.

3.1.5.2 CPU Fault

If the CPU does not control all the signals as it should it is likely to be defective.

3.2 Change LCD Contrast

To check the functionality of the contrast controlling circuitry, choose the LCD test from the service software. Choose any test picture and then the desired contrast value 0..255, where 0 is the darkest and the 255 the lightest.

3.3 Contrast Change OK?

Test if the contrast changing works at least with two different contrast values. If the contrast seems to be good in the middle, low and high of the tunable range, then proceed to 3.4 If the contrast does not change, or if the range bad, then proceed to 3.3.1

3.3.1 LCDPWM OK?

Test if the duty factor of the PWM output of the CPU (D130/pin134) is changing according to the value given in the LCD test with the service software. If the level of the LCDPWM is OK, and the duty factor is changing from 1/255 to 254/255 then proceed to 3.3.1.2, otherwise go to 3.3.1.1

3.3.1.1 CPU Fault

If the CPU does control the PWMOUT signal correctly, even though the signal is disconnected from the PDA power unit, then it is likely that the CPU is at fault.

3.3.1.2 Check PDA Power Unit

The LCDVEE output of the PDA power unit should change within the legal limits according to the PWMOUT signal duty factor. If the PWMOUT signal is controlled OK, but the LCDVEE voltage doesn’t change, then check the PDA power unit. Check components R86, C90 and R83.

3.4 Check LCD Test–Patterns

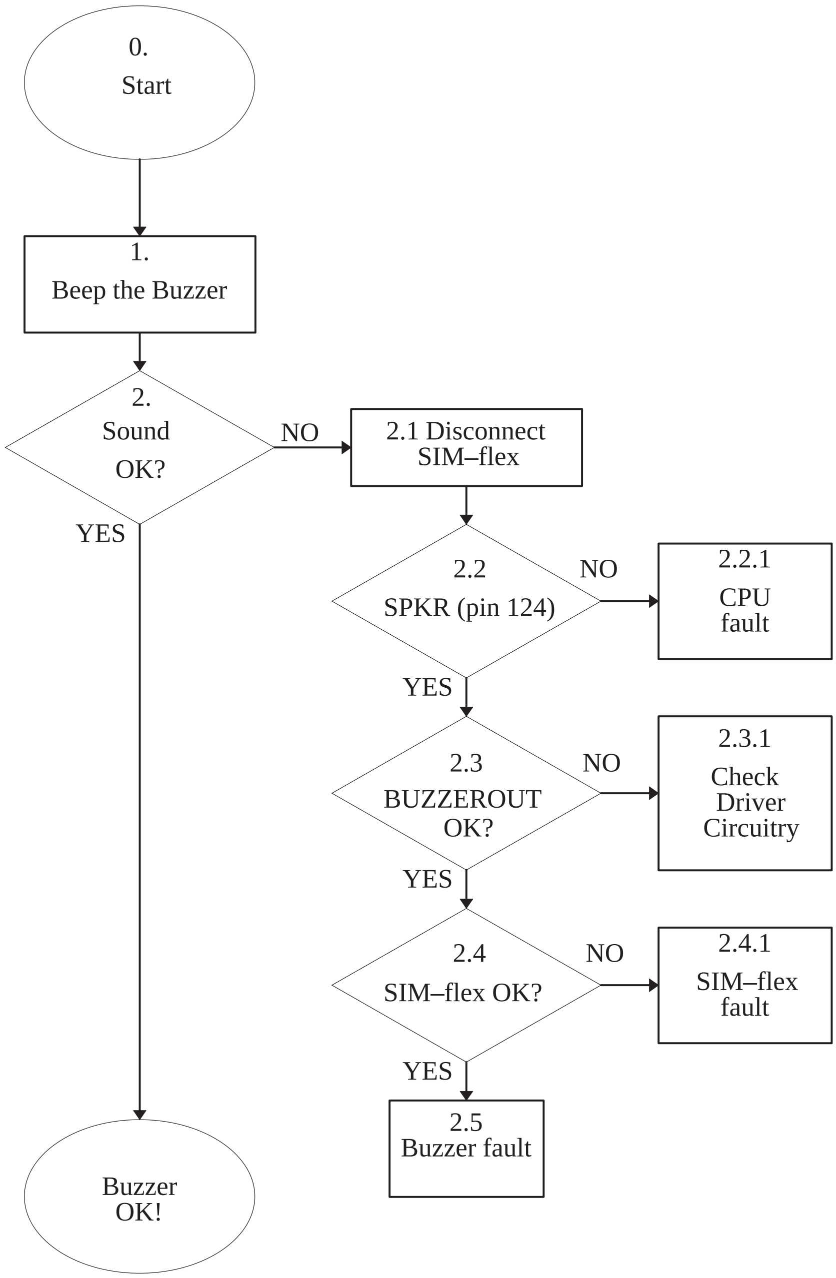
In order to check the functionality of every pixel on the LCD, various test patterns can be produced by selecting the LCD test in the service software.

3.5 Test–Patterns OK?

If all the pixels on the LCD toggle, the LCD test can be considered to have been successful. If there are some pixels / patterns that are not OK, then return to 3.1.4

4 Troubleshooting Diagram of the Buzzer

The functionality of the buzzer can be checked with the Service Software. The buzzer test tests the timer controls along with some other internal functions of the CPU.



4.1 Beep the Buzzer

To beep the buzzer, choose the buzzer test in the service software. Give the desired frequency and the duration.

4.2 Sound OK?

Listen to the sound, or optionally measure the output of the BUZZEROUT with an oscilloscope. If the frequency and the level are correct, then proceed to 4.2.1 otherwise the buzzer can be considered to be functional.

4.2.1 Disconnect SIM–Flex

In order to isolate the fault to the PDA module, disconnect the SIM–flex.

4.2.2 SPKR (pin 124)

Check the output of the pin 124 in the CPU (D130). Output should be a square wave at a given frequency. If the signal is not toggling, go to 4.2.2.1 If the CPU controls the output ok, then proceed to 4.2.3

4.2.2.1 CPU Fault

If the CPU does not control the SPKR output, even though the buzzer test is reported to be successful by the service software, then the CPU is likely to be faulty.

4.2.3 BUZZEROUT OK?

If the BUZZEROUT is OK then proceed to 4.2.4, otherwise the fault is in the buzzer driver circuitry; proceed to 4.2.3.1

4.2.3.1 Check Driver Circuitry

If the SPKR output stops before BUZZEROUT, check the circuitry R142–R148, V132–V135, C138.

4.2.4 SIM–Flex OK?

Check if the SIM–flex, and all the connectors are OK. If the connection from BUZZEROUT to the buzzer is OK, then proceed to the 4.2.5, otherwise go to 4.2.4.1

4.2.4.1 SIM–Flex Fault

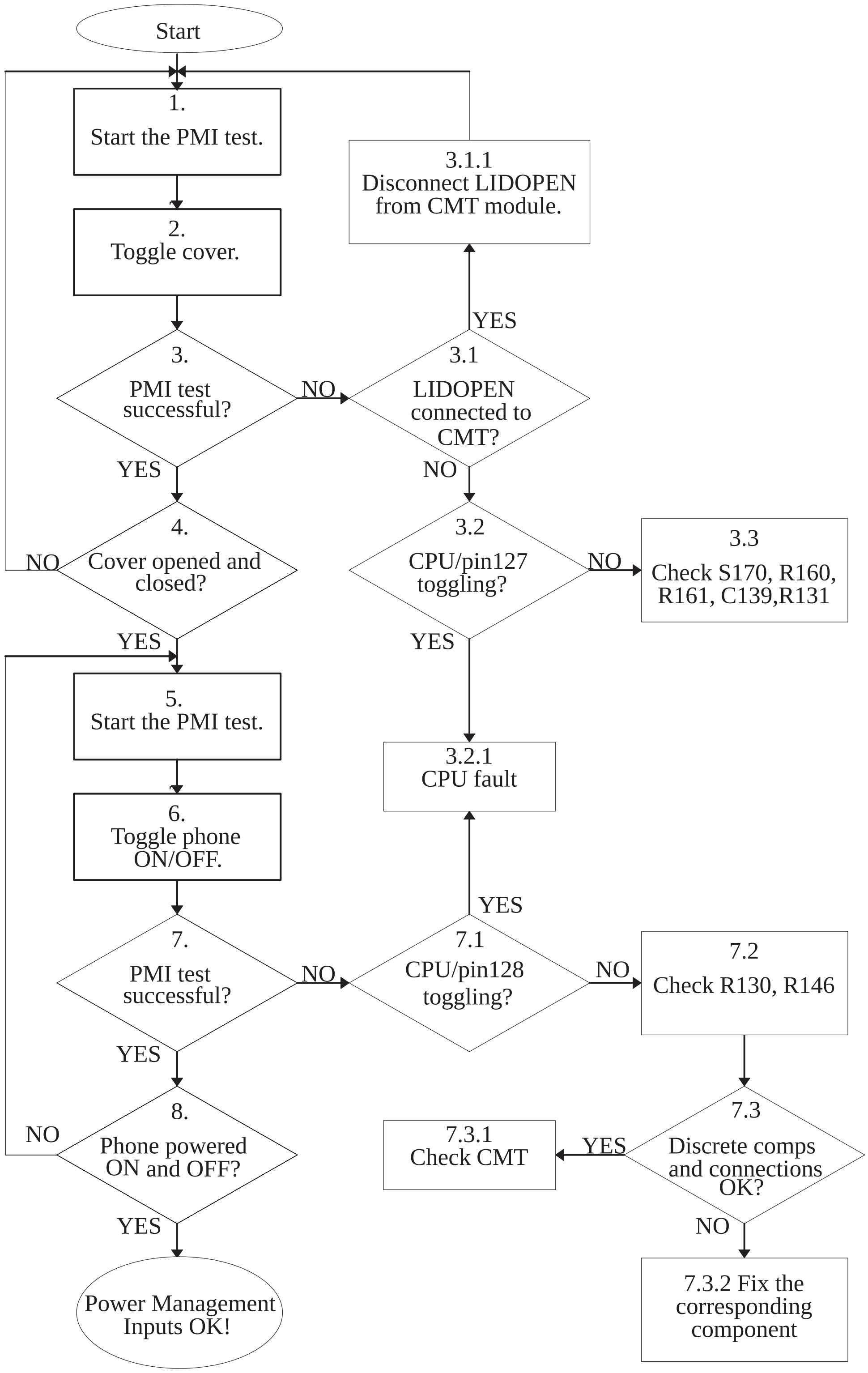
If the connection between the BUZZEROUT and the buzzer is broken, check the SIM–flex along with the board–to–board connectors, CMT module etc.

4.2.5 Buzzer Fault

If the CPU driven square wave is coming to the buzzer, but the buzzer does not beep, then change the buzzer.

5 Troubleshooting Diagram of the PMI Check

Once this test is activated the PDA waits for a power management interrupt to occur. The two possible sources for this interrupt are the lid–switch and the power switch of the CMT module.



5.1 Start the PMI Test

Start the PMI test by choosing the PMI test in the service software. Give a reasonable timeout value within which the interrupt is likely to occur.

5.2 Toggle Cover

In order to generate an interrupt, toggle the cover open or close.

5.3 PMI Test Successful?

If the service software reports the PMI test to been successful, proceed to 5.4 otherwise go to 5.3.1

5.3.1 LIDOPEN Connected to CMT?

In order to isolate the fault to the PDA module check if the LIDOPEN signal is connected to the CMT module. If the signal is connected go to 5.3.1.1 otherwise continue to 5.3.2

5.3.1.1 Disconnect LIDOPEN from the CMT Module

In order to isolate the fault to the PDA module, disconnect the CMT module. Proceed back to 7.1.

5.3.2 CPU pin 127 Toggling?

Check if the CPU pin 127 toggles according to the lid switch. The toggling can be checked by moving a magnet on the S170, or just by short circuiting it. If the pin does not toggle, then proceed to 5.3.3 otherwise go to 5.3.2.1

5.3.2.1 CPU Fault

If the CPU pin 127 (PMI0) or pin 128 (PMI1) is toggling while the PMI test is armed, and the PCLocals reports the test to have been unsuccessful, then it is likely that the CPU is not working correctly.

5.3.3 Check S170, R149, R150, R151, C139

If the signal is not toggling, change the faulty component.

5.4 Cover Opened and Closed?

Repeat the test switching the cover to the opposite position, i.e opened –> close and closed –> open. Goto 5.5

5.5 Start the PMI Test

Start the PMI test by choosing the PMI test in the service software. Give a reasonable time–out value within which the interrupt is likely to occur.

5.6 Toggle Phone ON/OFF

In order to generate an interrupt, toggle the CMT module ON or OFF.
***NOTE**: the CMT switches OFF several seconds after the power switch has been pressed!*

5.7 PMI Test Successful?

If the service software reports the PMI test to been successful, proceed to 5.8 otherwise go to 5.7.1

5.7.1 CPU pin 128 Toggling?

Check if the CPU pin 128 toggles according to the power ON/OFF switch of the CMT. If the pin does not toggle, then proceed to 5.7.2 otherwise go to 5.3.2.1

5.7.2 Check R130, R146

If the signal is not toggling, check the resistors.

5.7.3 Discrete Components and the Connections OK?

If the resistors and the connections to the CMT module are OK, proceed to 5.7.3.1 otherwise go to 5.7.3.2

5.7.3.1 Check CMT

If the resistors and the connections to the CMT module are OK, then the fault is in the CMT module.

5.7.3.2 Change the Corresponding Component

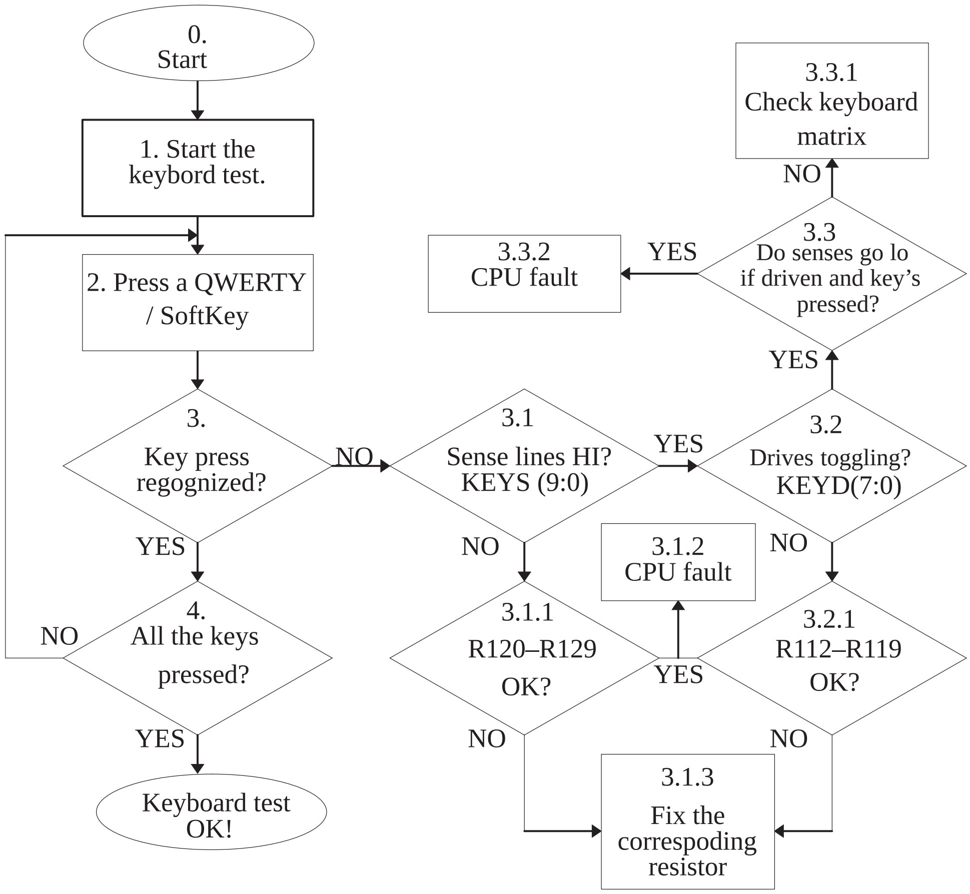
Change the bad resistor.

5.8 Phone Powered ON and OFF?

Do the test using both transitions phone OFF –> switch the phone ON, phone ON –> switch the phone OFF. If both transitions were successful, the PMI test can be considered to have been successful.

6 Troubleshooting Diagram of the Keyboard

The following picture illustrates the troubleshooting diagram of the keyboard. Once the keyboard test is started, all the keys of the PDA can be tested.



6.1 Start the Keyboard Test

Start the keyboard test with the service software. The test waits for a key–press within the given time period.

6.2 Press a QWERTY / Softkey

Press a key on the QWERTY keyboard or one of the soft–keys of the PDA.

6.3 Key Press Recognized?

If the key was recognized it prints the name of the key on the screen. If a legal combination of keys are pressed simultaneously, all the pressed keys are shown on the screen. If the key–press was not recognized then proceed to 6.3.1 otherwise go to 6.4

6.3.1 Sense Lines HI, KEYS (9:0)?

Pressing a key draws the sense line low, from idle high state, where it is connected in the keyboard matrix. Therefore, if no key is pressed, all the KEYS sense lines should be in a logic high state. Should this happen, continue to 6.3.2 otherwise proceed to 6.3.1.1

6.3.1.1 R120–R129 OK?

Check the sense line pull–ups. If the resistors are OK, then proceed to 6.3.1.2 otherwise go to 6.3.1.3

6.3.1.2 CPU fault

If the pull–ups R120–R129 are OK, then it is likely that the CPU (D130) is pulling the sense–line low. Expect a CPU fault.

6.3.1.3 Fix the Corresponding Resistor

Change the faulty resistor.

6.3.2 Drives Toggling KEYD(7:0)?

Once the keyboard test is running, it drives the keyboard drive lines from idle high to low state one by one, one at a time. if one or more line(s) remain fixed low or high, go to 6.3.2.1

6.3.2.1 R112–R119 OK?

The keyboard matrix is driven through the series resistors R112–R119. Check if all the resistors are OK. If the resistors are OK, go to 6.3.1.2 if not go to 6.3.1.3

NOTE: Resistors R112–R119 are installed only in CPU versions A3 or A5. If A7 version of the CPU is used, the resistors are not installed. Also if the A7 version of the CPU is used, then the value of the resistors R120–R129 is changed!

6.3.3 Do Senses Go Low if Driven and a Key Is Pressed?

Press a key in the matrix and scope the corresponding sense line. If the drive line is driven, but the sense line remains high proceed to 6.3.3.1 otherwise go to 6.3.3.2

6.3.3.1 Check keyboard matrix

If the sense line remains high, even though it should be forced low when driven, expect a fault on the circuit connections. Although the CPU can force the senses high also.

6.3.3.2 CPU Fault

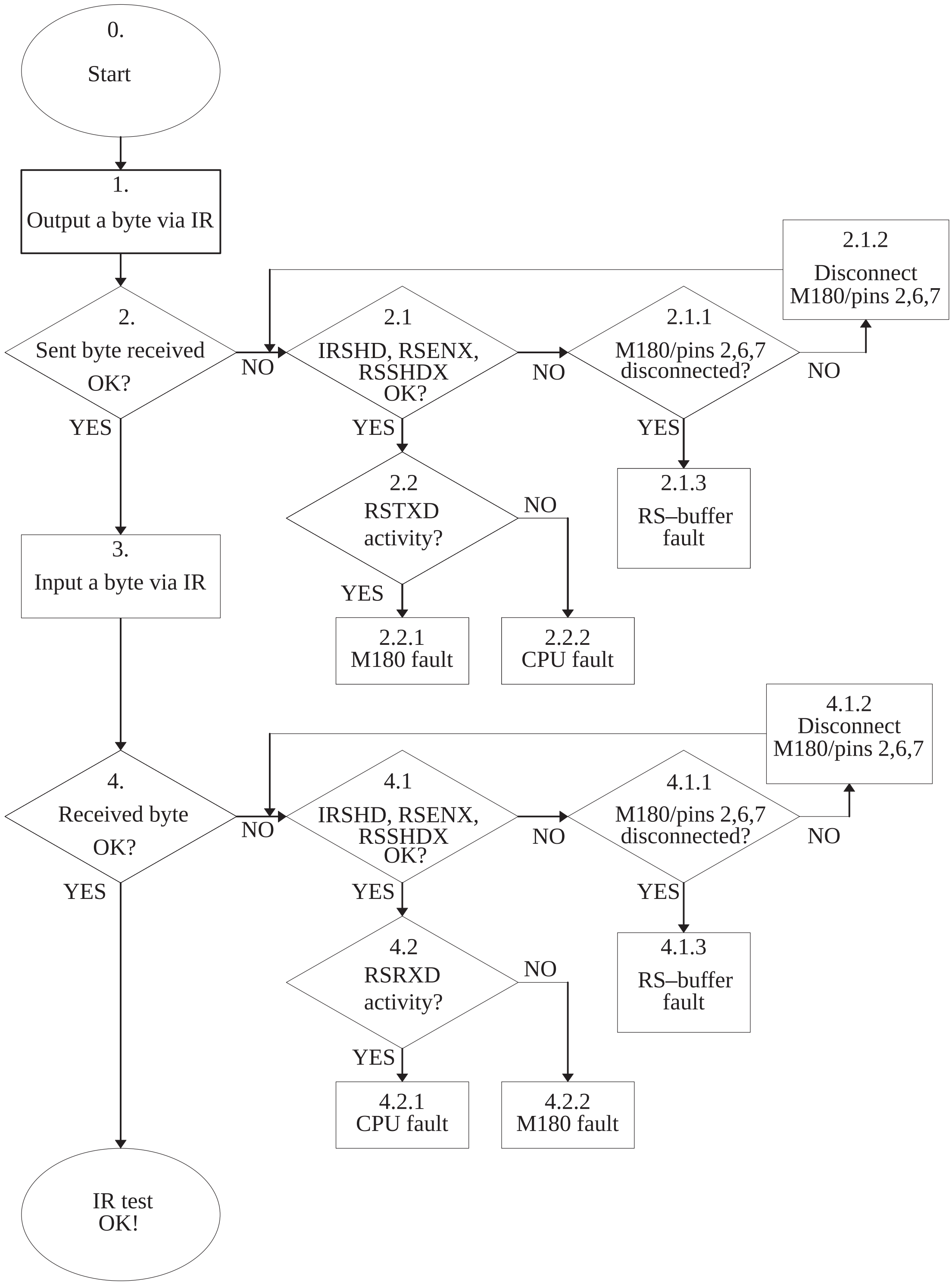
If the sense lines toggle according to the pressed keys on the keyboard when they are driven, then the CPU is likely to be defective.

6.4 All the Keys Pressed?

If all the keys are pressed, and they have been recognized correctly, the keyboard test can be considered to have been successful. If all the keys have not been tested, go back to 6.2

7 Troubleshooting Diagram of the InfraRed Check

The following picture illustrates the troubleshooting diagram of the infrared test. Only half duplex method is supported for testing the IR connection.



7.1 Output a Byte via IR

Start the IR test from the service software. Select output mode and the byte to send from the 9000. The external IR tranceiver should be connected to the other serial port, where the DLR–1 cable is connected.

7.2 Sent Byte Received OK?

If the service software can receive the byte sent, continue to 7.3 otherwise proceed to 7.2.1

7.2.1 IRSHD, RSENX, RSSHDX OK?

When the byte is sent, it toggles the RSENX from logic low to high, RSSHDX at the same time from logic high to low, and after few milliseconds the IRSHD from logic high to low. If these signals do not toggle correctly, proceed to 7.2.1.1 If the signals are OK, then go to 7.2.2

7.2.1.1 M180 / pins 2,6,7 Disconnected?

To isolate a problem with the IRSHD, RSENX and the RSSHDX that does not control the RS–buffer and the M180 IR tranceiver module correctly, disconnect the control signals from the M180. If the pins are connected continue to 7.2.1.2, otherwise go to 7.2.1.3

7.2.1.2 Disconnect M180 / pins 2,6,7

By doing this, the control signals can be isolated to the RS–buffer or to the CPU. Go back to 7.2.1

7.2.1.3 RS–Buffer Fault

If the control signals do not toggle to the right state, even though the IR tranceiver is isolated, then the fault is most likely in the RS–buffer (D180). However it is possible, that the CPU does not control the lines. But since the RS–buffer is needed for the communications to the host, it can not be tested, if the control signals are disconnected between the CPU – RS–buffer.

7.2.2 RSTXD Activity?

If the byte is already sent to the IR tranceiver, then the RSTXD line toggles immediately after the control signals are toggled. If the RSTXD signal toggles proceed to 7.2.2.1 otherwise go to 7.2.2.2

7.2.2.1 M180 Fault

If all the signal lines to the IR tranceiver toggle as they should, the M180 is likely to be faulty.

7.2.2.2 CPU Fault

If the RSTXD signal does not toggle, then the CPU is likely to be faulty.

7.3 Input a Byte via IR

If the sending of a byte was successful, try then to receive one. Choose the Input mode in the service software, and choose a byte to be received.

7.4 Received Byte OK?

If the service software reports success, the IR test can be considered to have been successful, otherwise proceed to 7.4.1

7.4.1 IRSHD, RSENX, RSSHDX OK?

When the 9000 begins to receive the byte, it toggles the RSENX from logic low to high, RSSHDX at the same time from logic high to low, and after few milliseconds the IRSHD from logic high to low. If these signals do not toggle correctly, proceed to 7.4.1.1 If the signals are OK, then go to 7.4.2

7.4.1.1 M180 / pins 2,6,7 Disconnected?

To isolate a problem with the IRSHD, RSENX and the RSSHDX that does not control the RS–buffer and the M180 IR tranceiver module correctly, disconnect the control signals from the M180. If the pins are connected continue to 7.4.1.2, otherwise go to 7.4.1.3

7.4.1.2 Disconnect M180 / pins 2,6,7

By doing this, the control signals can be isolated to the RS–buffer or to the CPU. Go back to 7.4.1

7.4.1.3 RS–Buffer Fault

If the control signals do not toggle to the right state, even though the IR tranceiver is isolated, then the fault is most likely in the RS–buffer (D180). However it is possible, that the CPU does not control the lines. But since the RS–buffer is needed for the communications to the host, it can not be tested, if the control signals are disconnected between the CPU – RS–buffer.

7.4.2 RSRXD Activity?

If the byte is received by the IR tranceiver, then the RSRXD line toggles right after the control signals are toggled. If the RSRXD signal toggles proceed to 7.4.2.1, otherwise go to 7.4.2.2.

7.4.2.1 CPU Fault

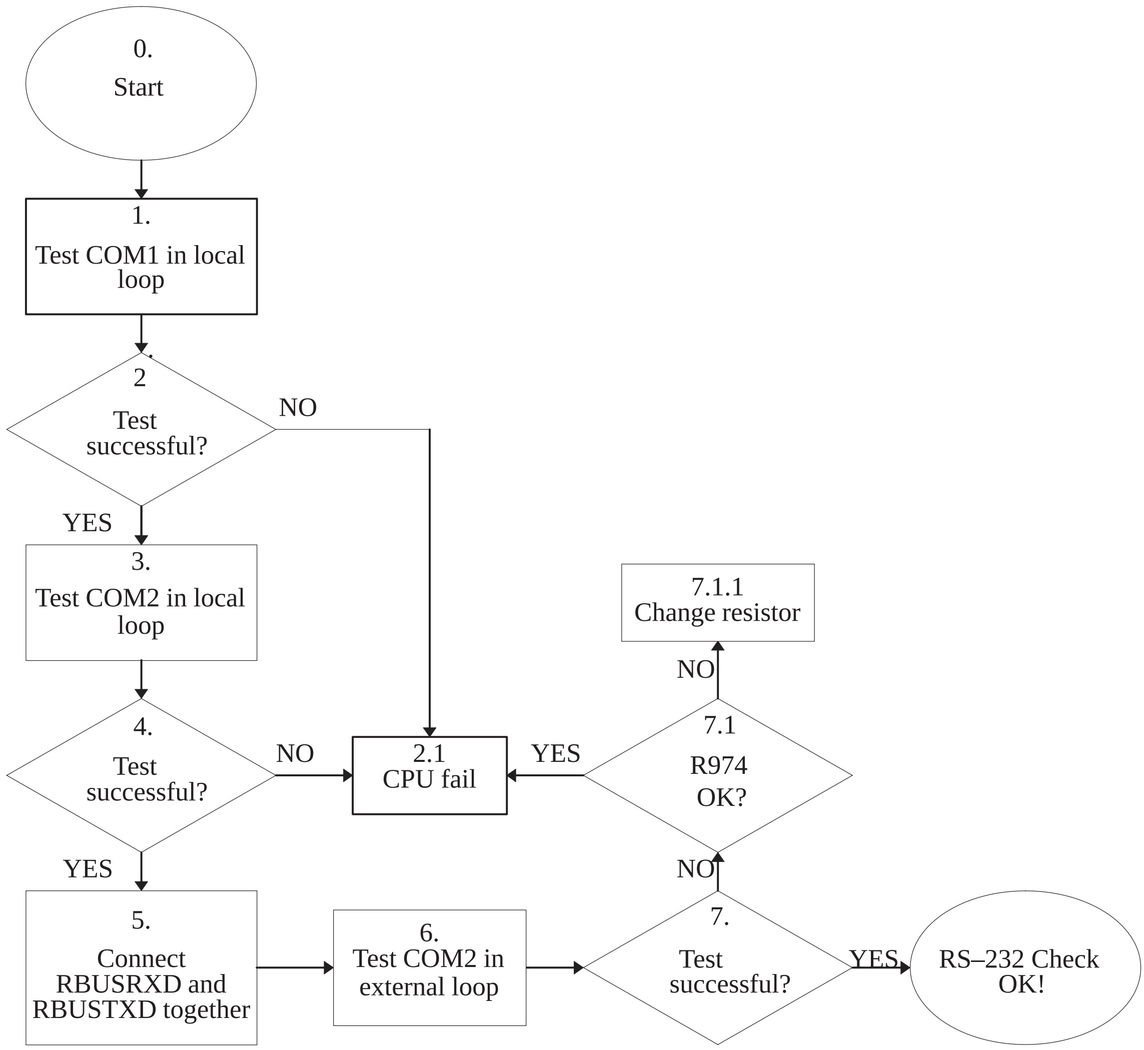
If all the signal lines to the IR tranceiver toggle as they should, and there is activity in the RSRXD while the IR transmitter connected to the host PC is transmitting the byte, then the CPU is likely to be faulty.

7.4.2.2 M180 Fault

If the RSRXD signal does not toggle, then the M180 is likely to be faulty.

8 Troubleshooting Diagram of the RS–232 Check

The following picture illustrates the serial port tests. As the COM1 is being tested automatically in the communications to the host PC, only the COM2 can be tested externally with the aid of the service software. Both serial ports can be tested in the UART's local loop.



8.1 Test COM1 in Local Loop

Choose the serial test in the service software and select COM1 to be tested in a local loop. The test is ran at the same baud rate that is used in the communications to the host PC.

8.2 Test Successful?

If the test passes successfully proceed to 8.3, otherwise branch to 8.2.1

8.2.1 CPU Fault

If either of the tests in the local loop mode fails, then the CPU is defective.

8.3 Test COM2 in Local Loop

Select the COM2 to be tested in the local loop. The test is ran at 9600 baud by default.

8.4 Test Successful?

If the test passes successfully proceed to 8.5, otherwise branch to 8.2.1

8.5 Connect RBUSRXD and RBUSTXD Together

In order to test the external lines of the COM2, the RBUSRXD and RBUSTXD may be connected together e.g. in the board–to–board connector. When testing the COM2 in this external loop, the bytes are received via this connection.

8.6 Test COM2 in External Loop

Choose in the service software the COM2 test in external loop.

8.7 Test Successful?

If the test passes in the external loop, the serial ports can be considered to be functional, otherwise continue to 8.7.1

8.7.1 R947 OK?

There is only one resistor between the CPU pins 97–98, check it along with the connections. If OK, go to 8.2.1, if not go to 8.7.1.1.

8.7.1.1 Change Resistor

Change the faulty R974.

Appendix A

POST beep codes, number of beeps:

1	Memory refresh is not working.
3	Memory failure in 1st 64KB of memory.
4	Timer T1 not operational.
5	CPU test failed.
6	Gate A20 failure.
10	CMOS shutdown register failed.
13	Exhaustive low memory test failed.
14	Exhaustive extended memory test failed.
15	CMOS restart byte can’t hold data.
16	Address line test failed.
18	Interrupt controller failure.

Appendix B

POST progress codes. These are written during POST to the IO address 2FFh, and if the BIOS–testmode is entered the last code is copied to the IO address 3FFh.

00h	POST beginning
01h	CPU register test starting
05h	Disabling shadowing & cache
0Dh	Test CMOS RAM shutdown register
0Eh	Check CMOS checksum, update DIAG byte
11h	Disable interrupts controllers
12h	Disable Port B and video display
13h	Initialize chipset and start auto memory detect
15h	Test 8254 Timer2 for speaker, Port B
16h	Test 8254 Timer1 for refresh
17h	Test 8254 Timer0 for 18.2Hz
18h	Start memory refresh
1Ah	Test 15 us refresh ON/OFF time
19h	Test memory refresh
20h	Test address lines
22h	Base 64kB memory read/write test
23h	System initialization before vector table init
24h	Initialize vector table
35h	Check ROM BIOS data area at segment 40h
40h	Prepare virtual memory test, verify from display memory
42h	Enter virtual mode for memory test
44h	Initialize data for checking wraparound at 0:0
4Ch	Clear extended memory for soft reset
4Dh	Save memory size
53h	Save registers & memory size, enter real–mode
55h	Disable A20 line
66h	Initialize interrupt controllers
82h	Initialize circular buffer
84h	Check for memory size mismatch (CMOS/BIOSDATA)
8Fh	Configure floppy drives
94h	Set base & extended memory sizes
95h	Memory size adjusted for 1k, verify display memory
96h	Initialization before calling C800h
97h	Call ROM BIOS extensions at C800h
98h	Processing after extension returns
99h	Configure timer data area
A6h	Enable NMIs

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Chapter 9

Service Tools

CONTENTS –Service Tools

Introduction

This chapter outlines the service tools and accessories required for the Nokia 9000 Communicator.

Table 1. Service Tools and Accessories

Name	Type code	Material code	Notes , reference to material list
Dummy Test Battery	BTD–1	0770071	Without actual battery and with sense lines
Module Jig	MJS–1	0770076	
Carkit Jig	HCR–1	0770074	
Carkit Dummy Test Battery	BTD–1C	0770072	
Assembly jig	AJS–1	0770075	
Hinge Flex Insertion Pliers	PFH–1	0770078	
SIM Flex Insertion Pliers	PFS–1	0770077	
LCD Flex Insertion Pliers	PFL–1	0770079	
Modified Power Adapter	PAS–1	0770073	Used to activate test mode on GP1
Modular power Connector	SCF–6	0770036	
RS232 cable	DLR–1	0730077	
Software Protection Key	PKD–1	0750018	
Flash Programming Set	FPS–3	0270074	For GE8 Flash download.
Audio cable	ADS–1	0730011	
PC link adapter	DAU–2	0750006	
Connector cable	XCM–1	4626131	
Module T adapter		4626134	
D9/D25 RS232 Adapter		4626170	
The following tools are not illustrated			
LCD Flex Insertion Tweezers	TWL–1	0770080	
IR – RS232 adapter	RTA–1		
JTAG Flash download Set	FDS–1		
Multi–Responder Flash downl.	RDS–1		
BNC/MINI–UHF adapter		0198551	
B2B Measurement adapter	RBM–1	0775068	
B2B Hinge flex measure adapter	RBM–2	0775069	

Table 2. Service Kit

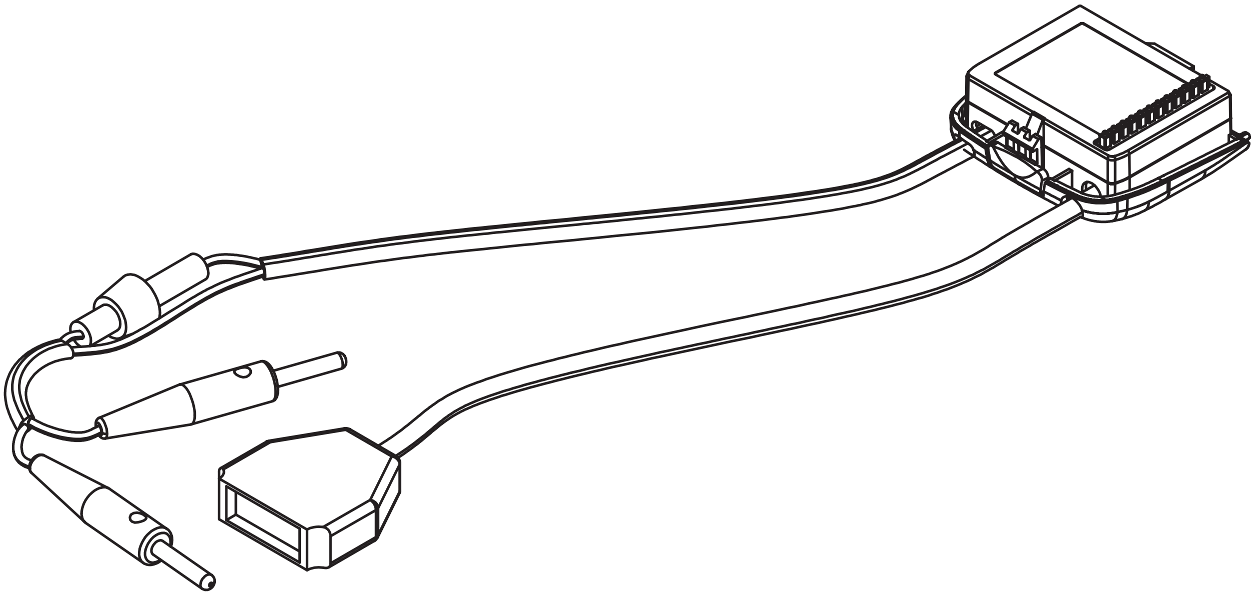
9000 Service Kit	*PFT–1K*	*0067041*	*Contents*
			Hinge Flex Insertion Pliers PFH–1
			SIM Flex Insertion Pliers PFS–1
			LCD Flex Insertion Pliers PFL–1
			LCD Flex Insertion Tweezers TWL–1

Table 3. Service Software configurations

RAE–1N Software	Service	0774057	1 x 3”disk
	CMT MCU	0775063	1 x 3”disk
English	PDA MCU	0775064	2 x 3”disk
German	PDA MCU	0775065	2 x 3”disk
French	PDA MCU	0775066	2 x 3”disk
Scandinavian	PDA MCU	0775067	2 x 3”disk

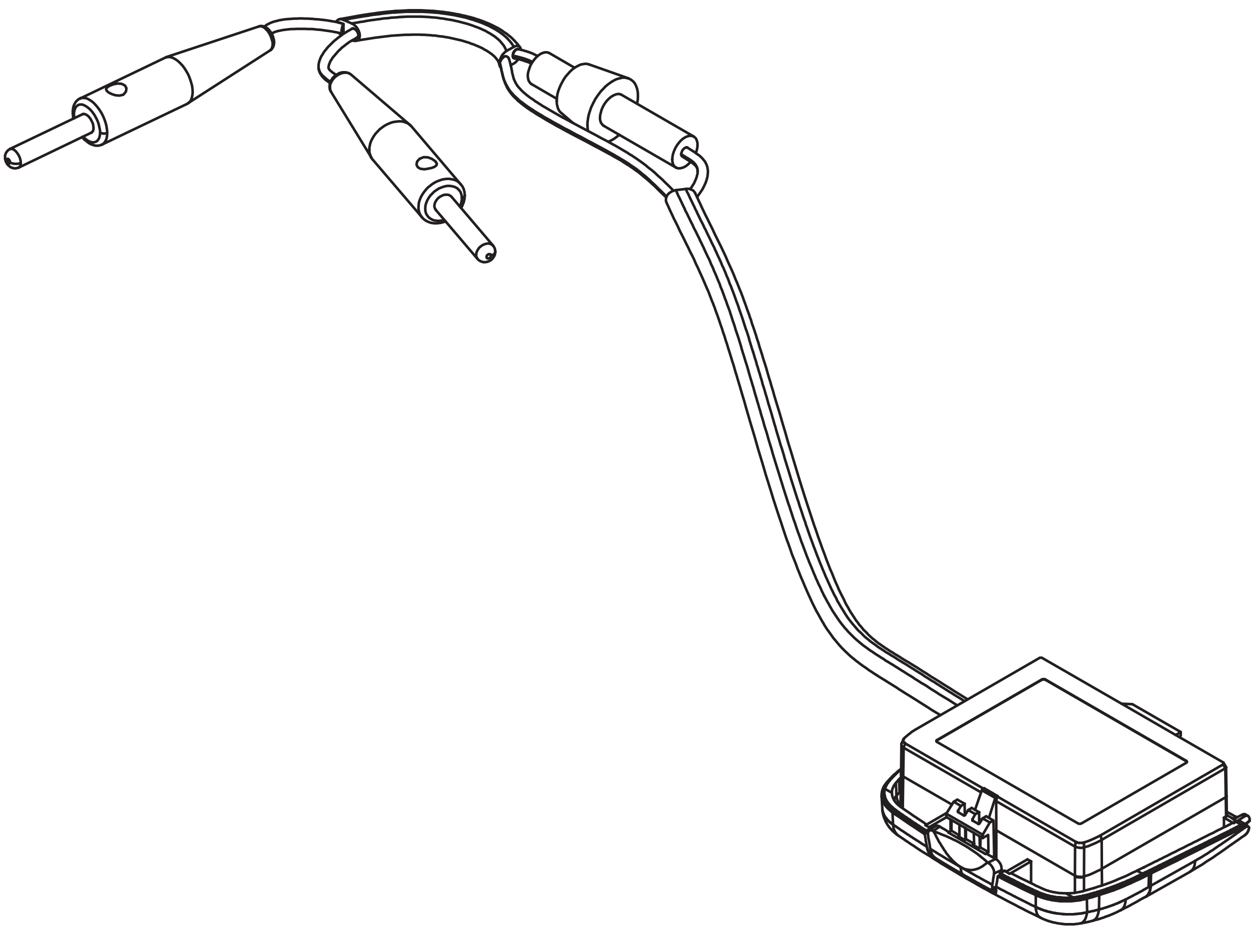
BTD –1 (Battery Test Dummy)

Material Code 0770071



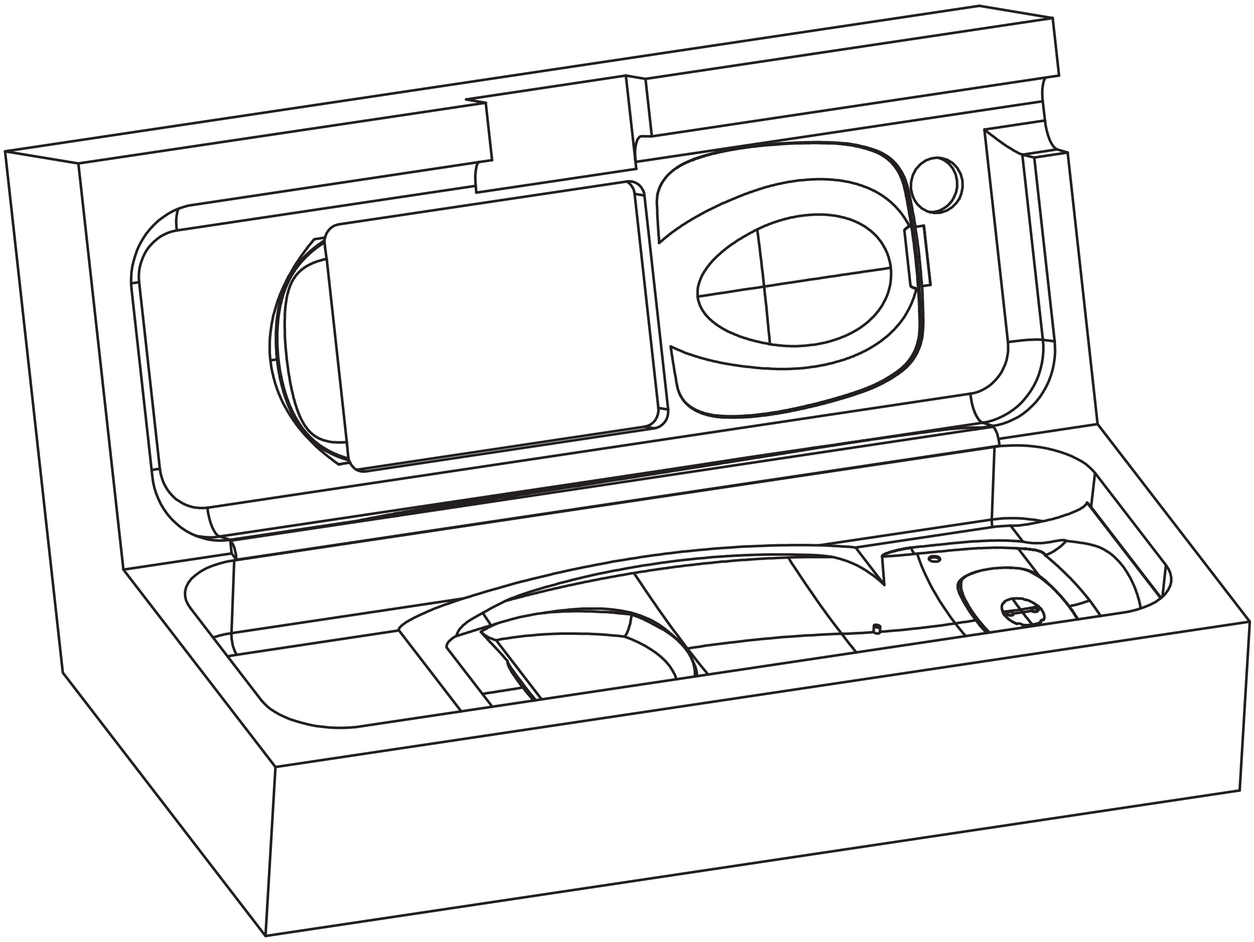
BTD –1C (Battery Test Dummy–Car kit)

Material Code: 0770072



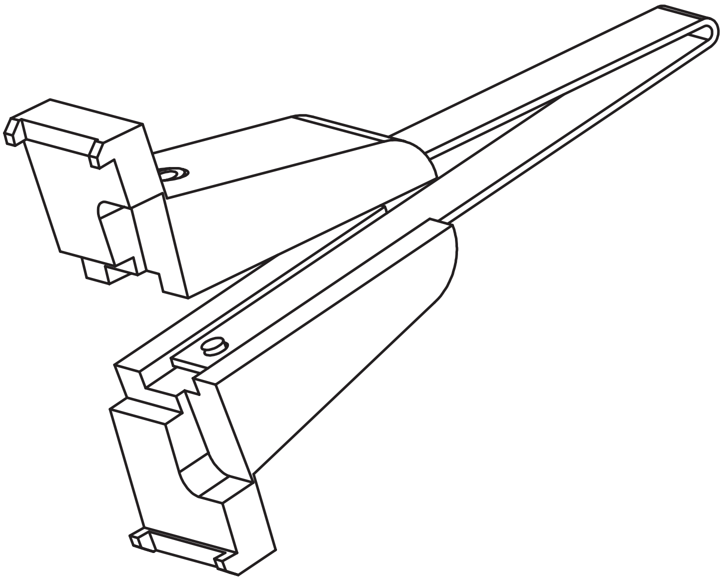
AJS–1 (Assembly Jig)

Material Code: 0770075



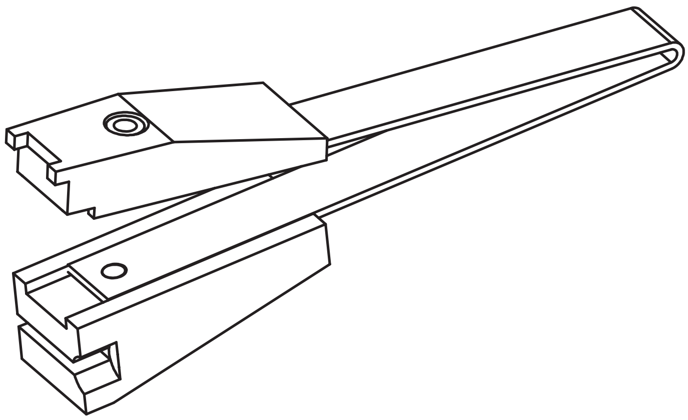
PFH–1 (Hinge Flex Insertion Pliers)

Material Code: 0770078



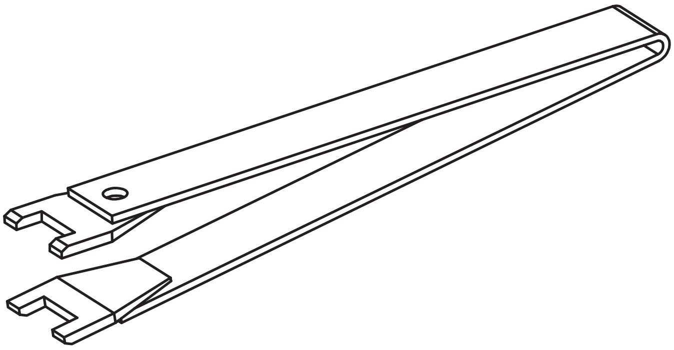
PFS–1 (SIM Flex Insertion Pliers)

Material Code: 0770077



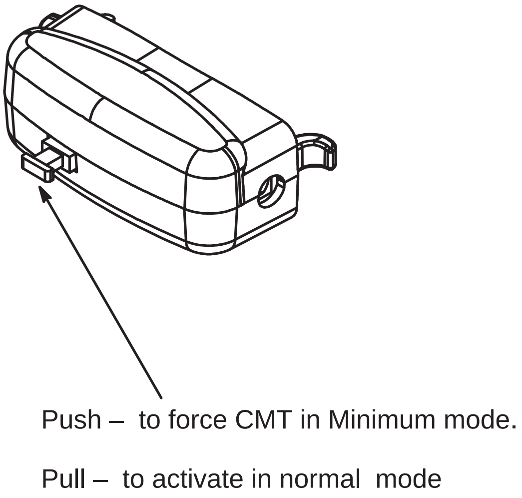
PFL–1 (LCD Flex Insertion Pliers)

Material Code: 0770079



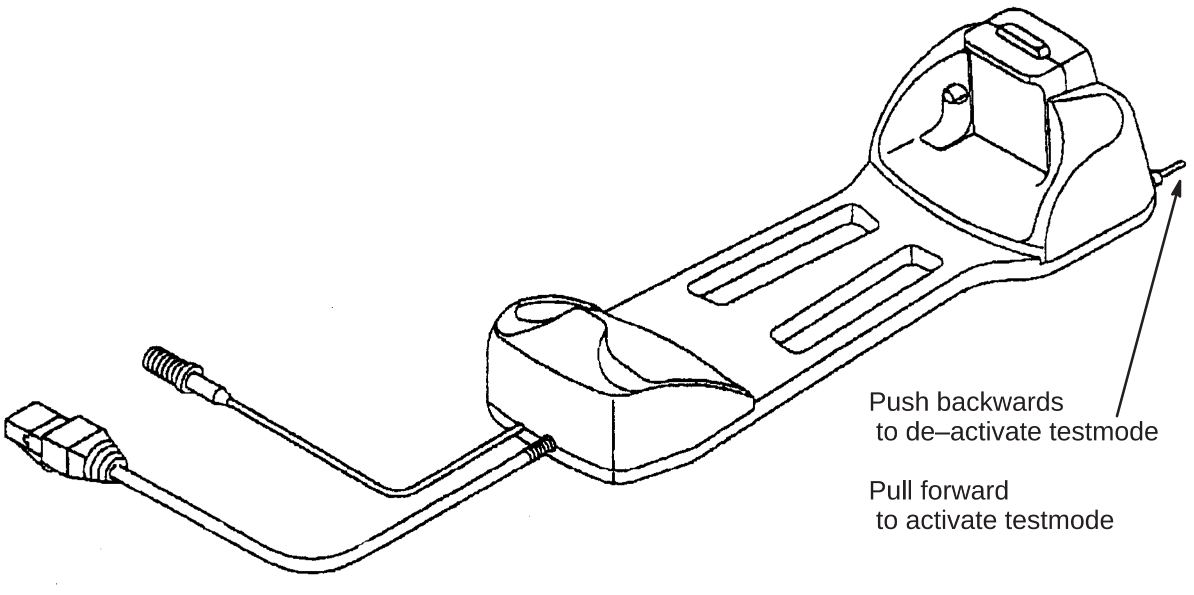
PAS–1 (Modified Power Adapter)

Material Code: 0770073



HCR–1 (Carkit Jig)

Material Code: 0770074

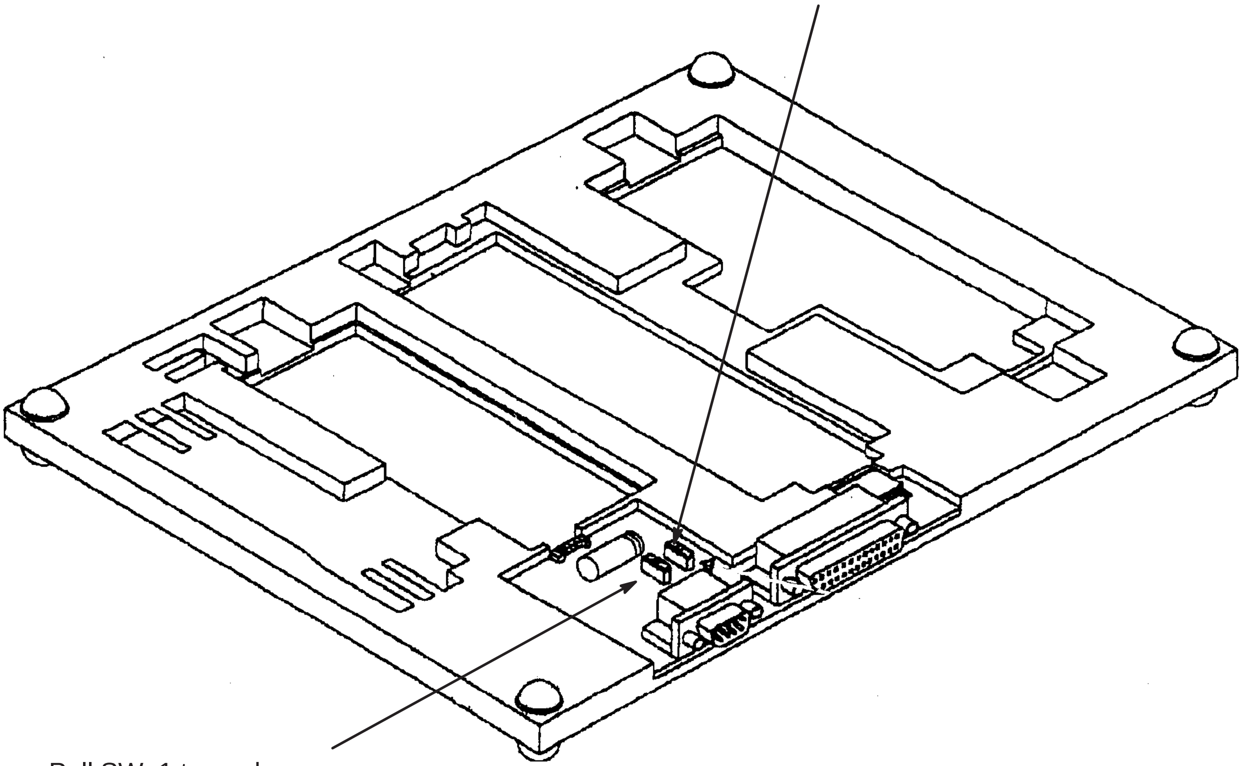


MJS–1 (Module Jig)

Material Code: 0770076

Pull SW–2
to activate PDA testmode

Push SW–2
to de–activate PDA testmode

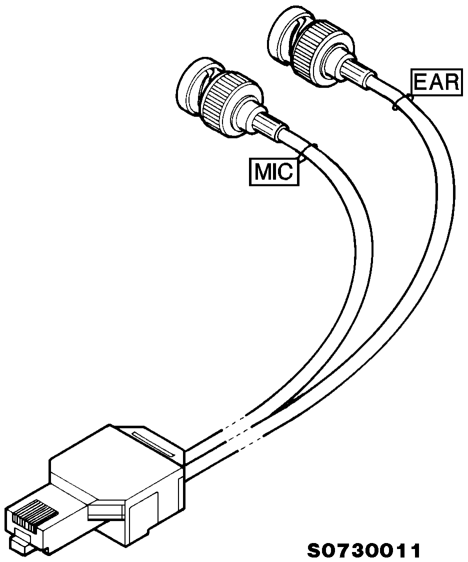


Pull SW–1 towards you
to activate charging

Push SW–1 away from you
to de–activate charging

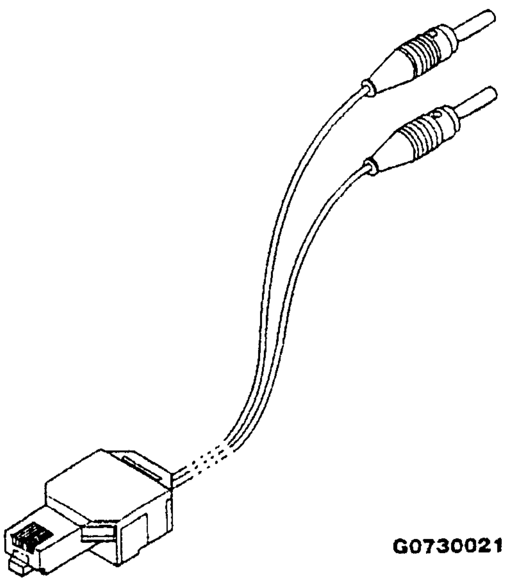
ADS–1 (Audio Cable)

Material Code: 0730011



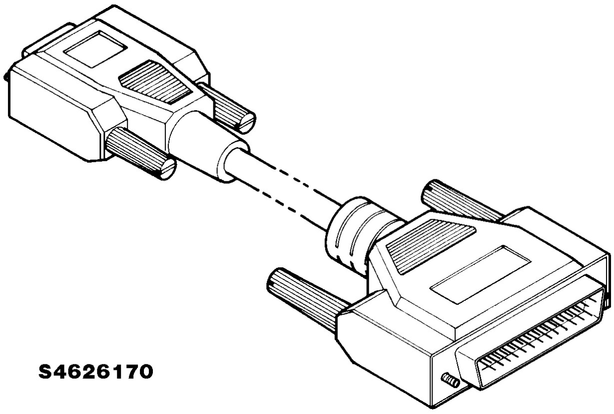
SCF–6 (Modular Power Connector)

Material Code: 0770036



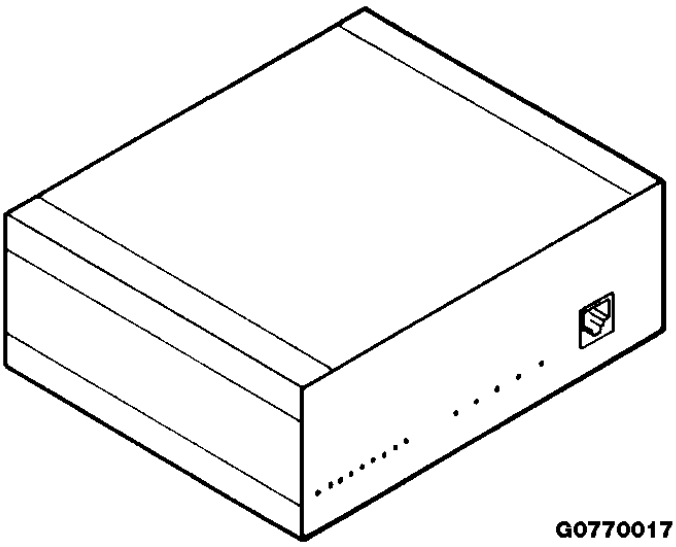
D9 – D25 RS232 Adapter

Material Code: 4626170



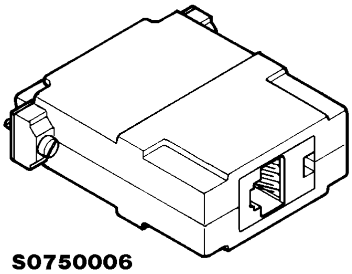
FPS–3 (Programmer)

Material Code: 0270074



DAU–2 /2T (PC Link Adapter)

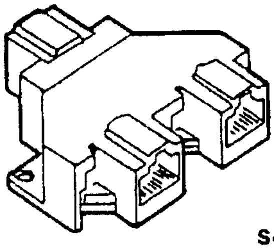
Material Code: 0750006



S0750006

Modular T adapter (Branch Connector)

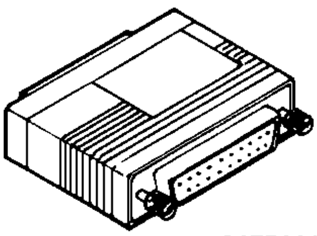
Material Code: 4626134



S4626134

PKD–1 Dongle (Software Protection Key)

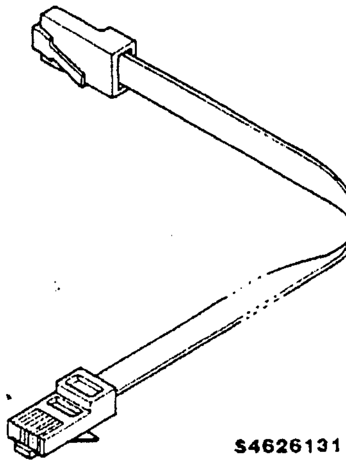
Material Code: 0750018



G0750018

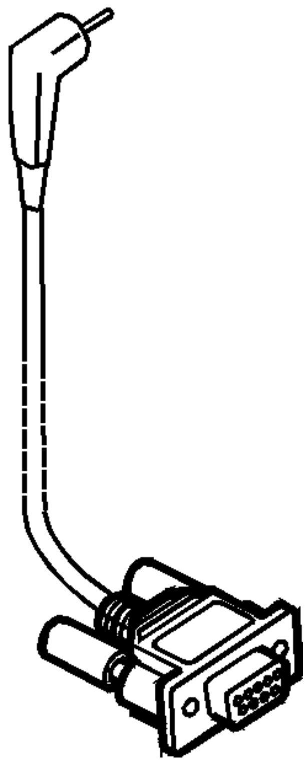
XCM–1 (Connector Cable)

Material Code: 4626131



DLR–1 (RS232 – 9000 Connector)

Material Code: 0730077



Chapter 10

Schematics

CONTENTS– Schematics

Figure 1. Component Layout – Bottom

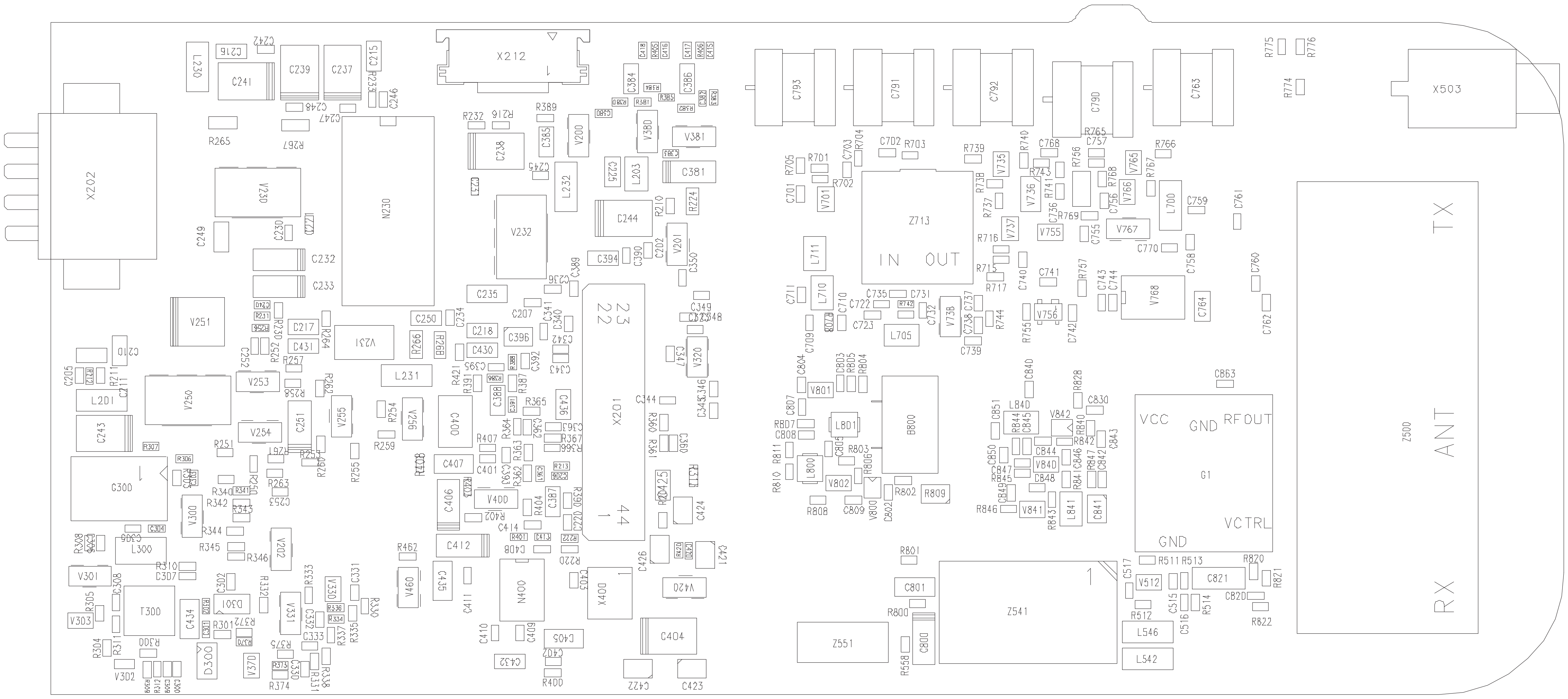


Figure 2 Component Layout – Top

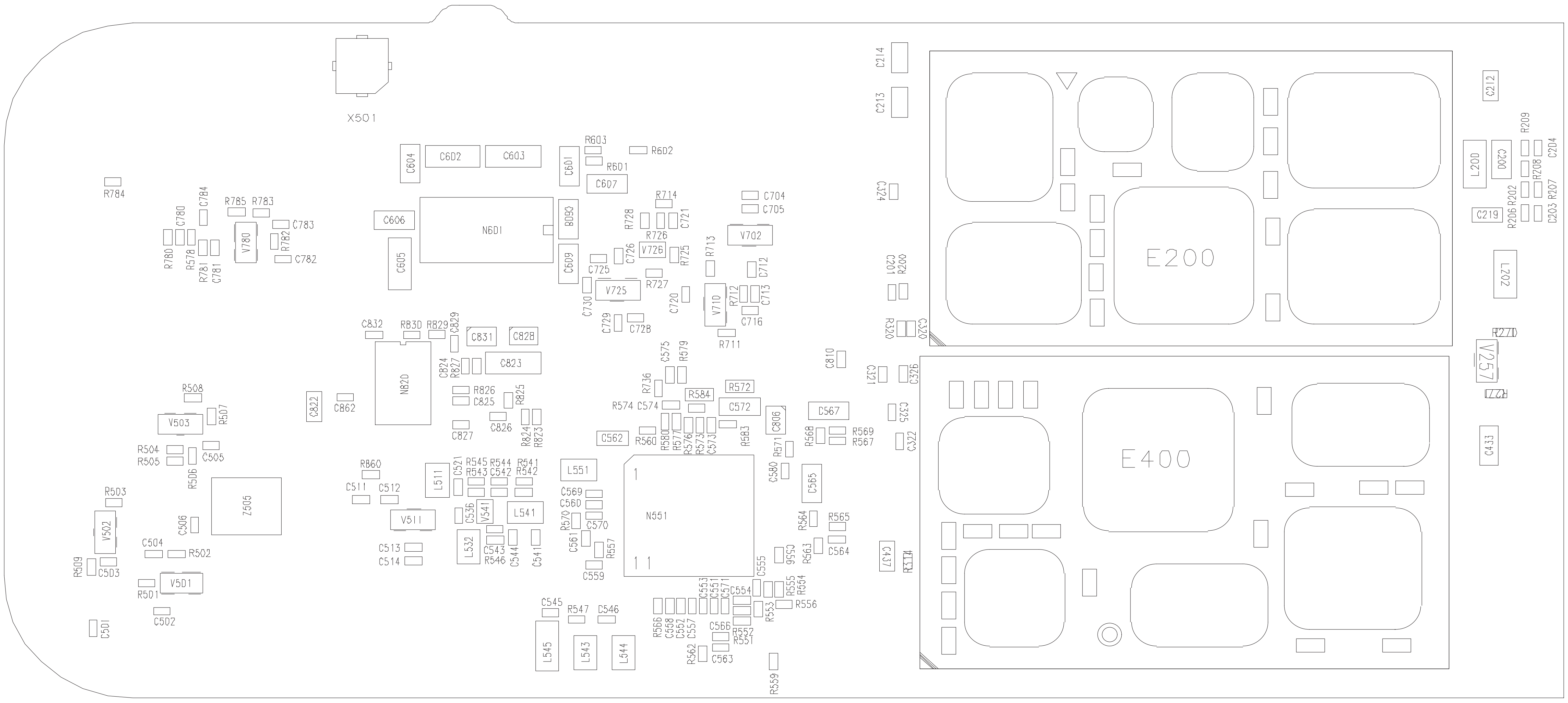


Figure 3 Baseband Circuit Diagram – PWRU

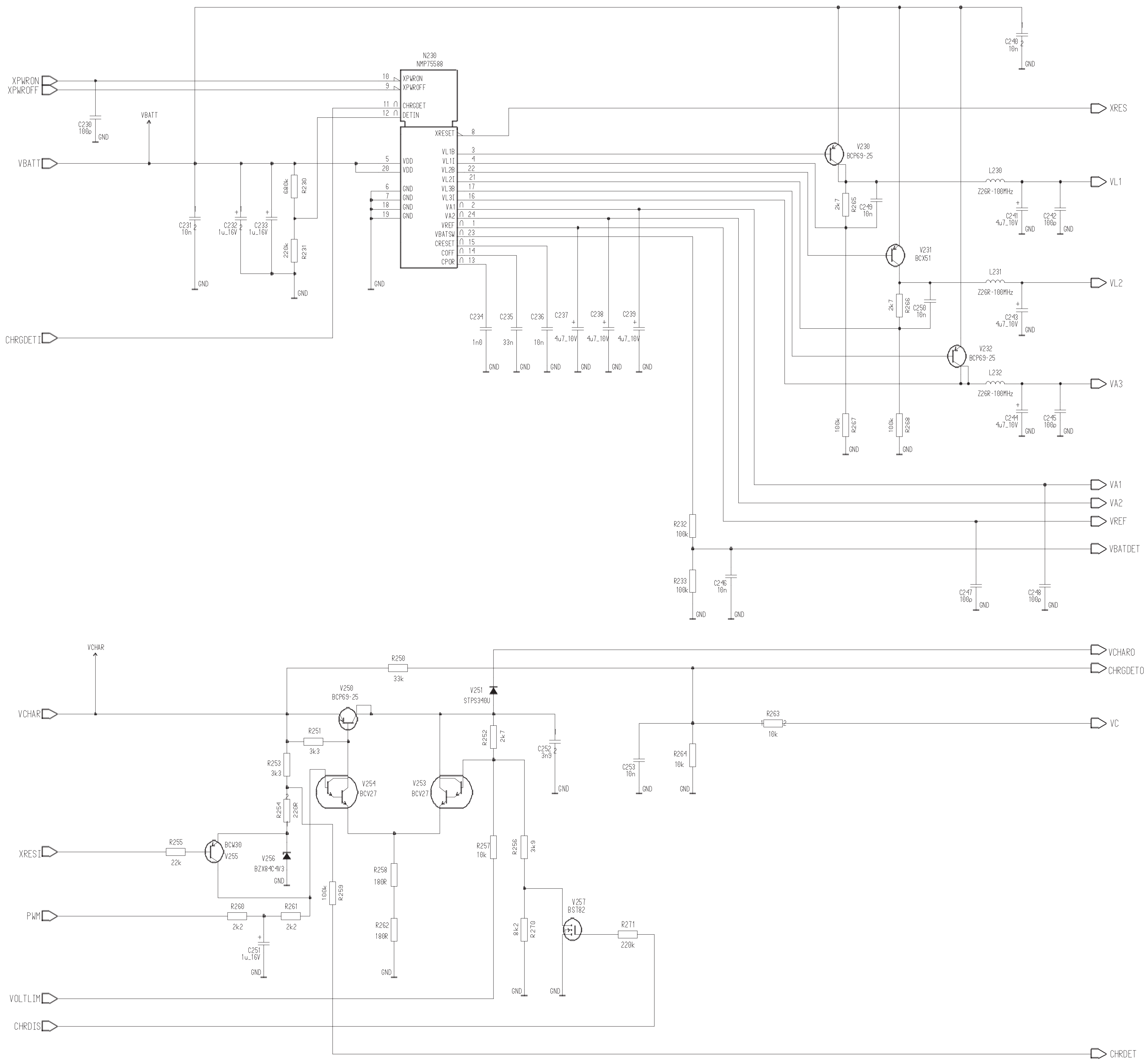


Figure 4 Baseband Circuit Diagram – MCM1

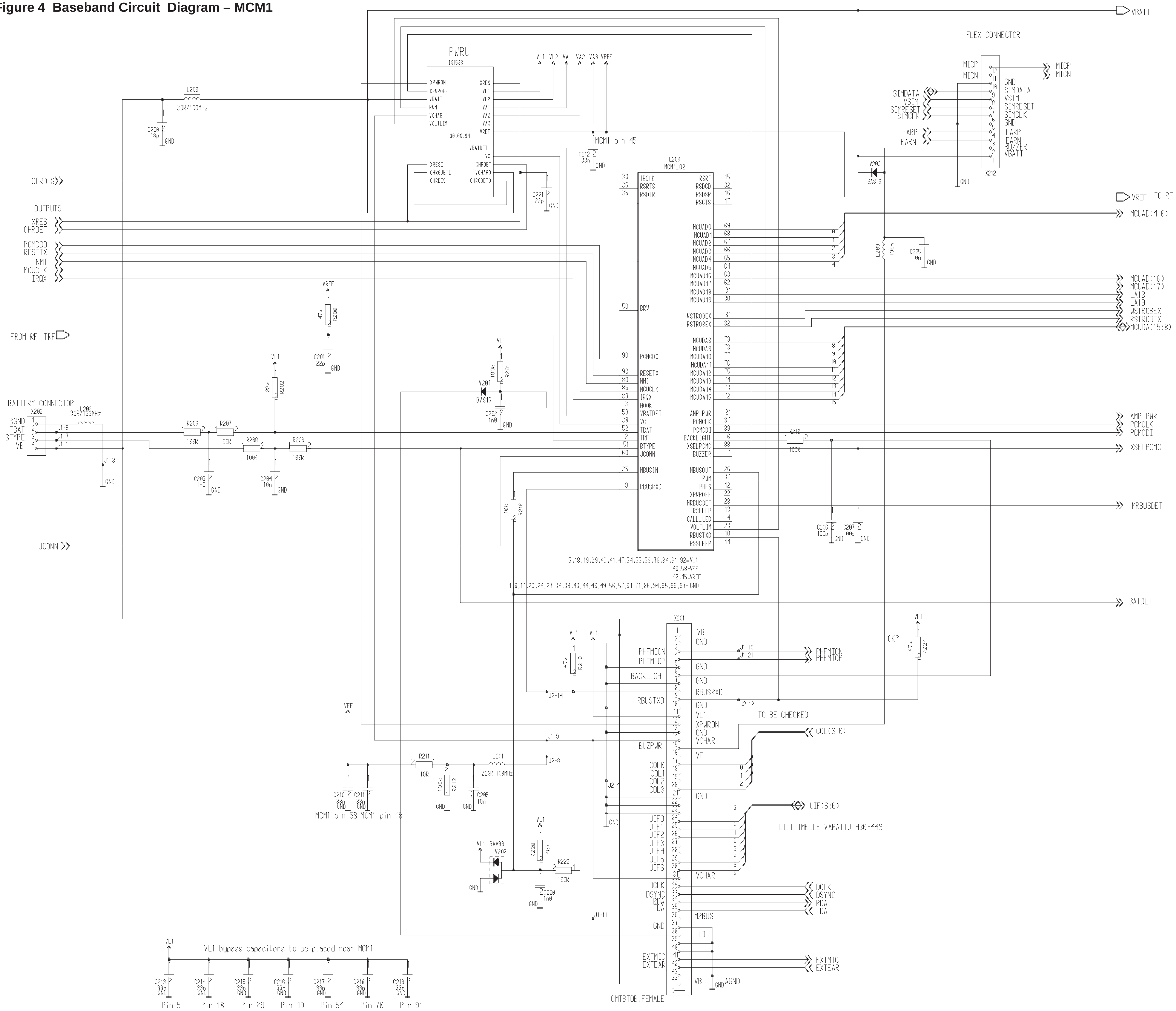


Figure 5 Baseband Circuit Diagram – MCM2

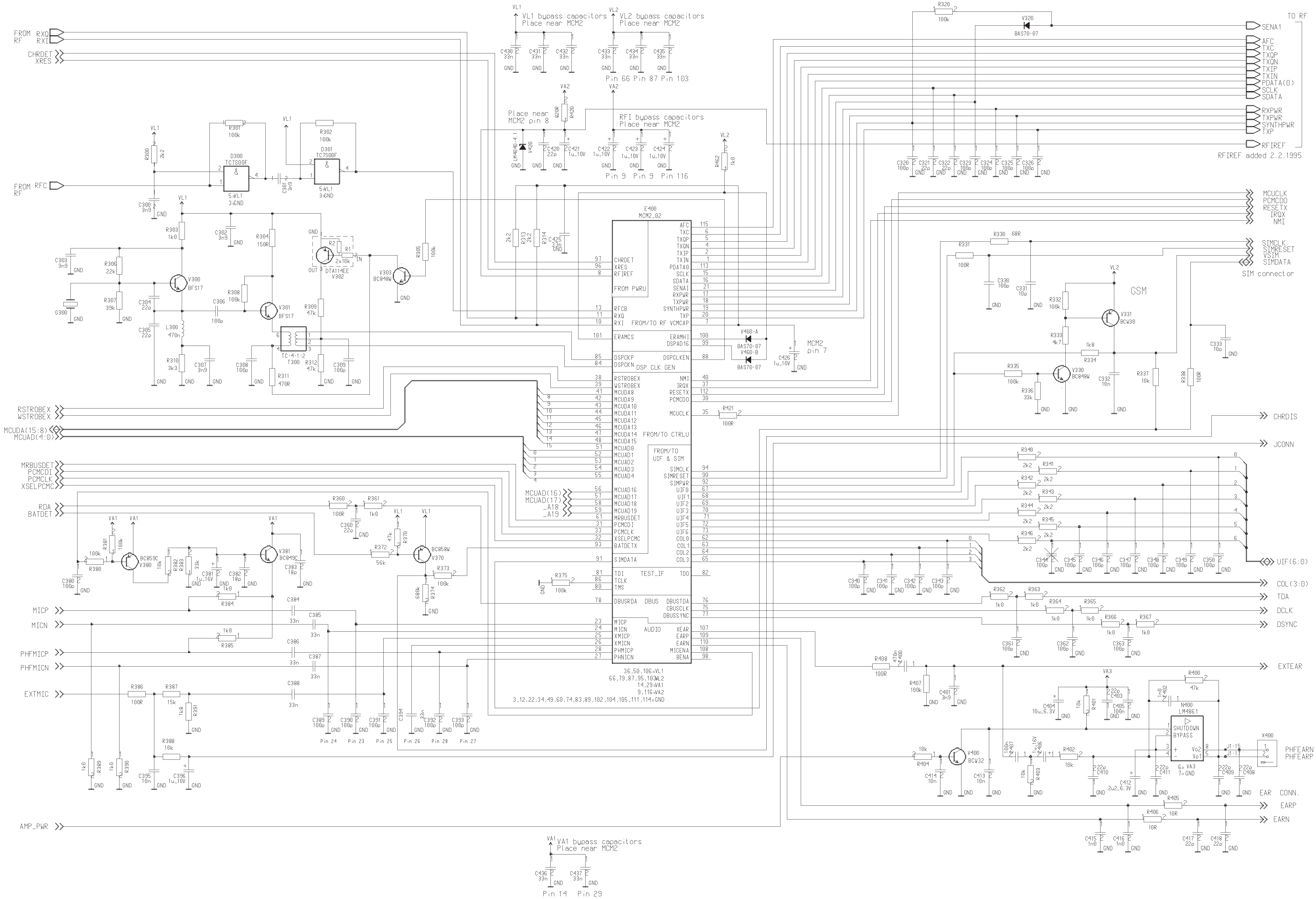


Figure 6 RF / TX Circuit Diagram

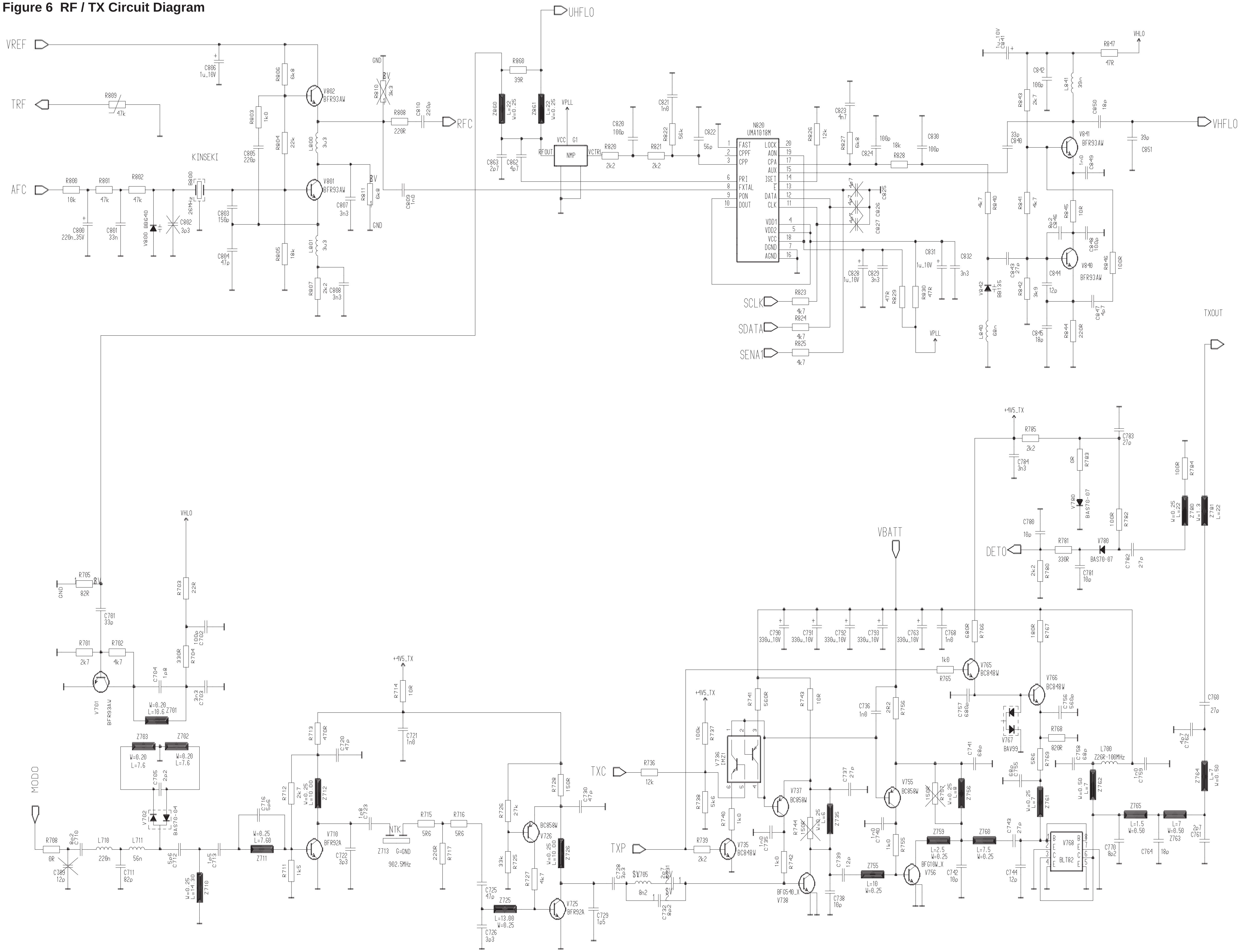


Figure 7 RF / RX Circuit Diagram

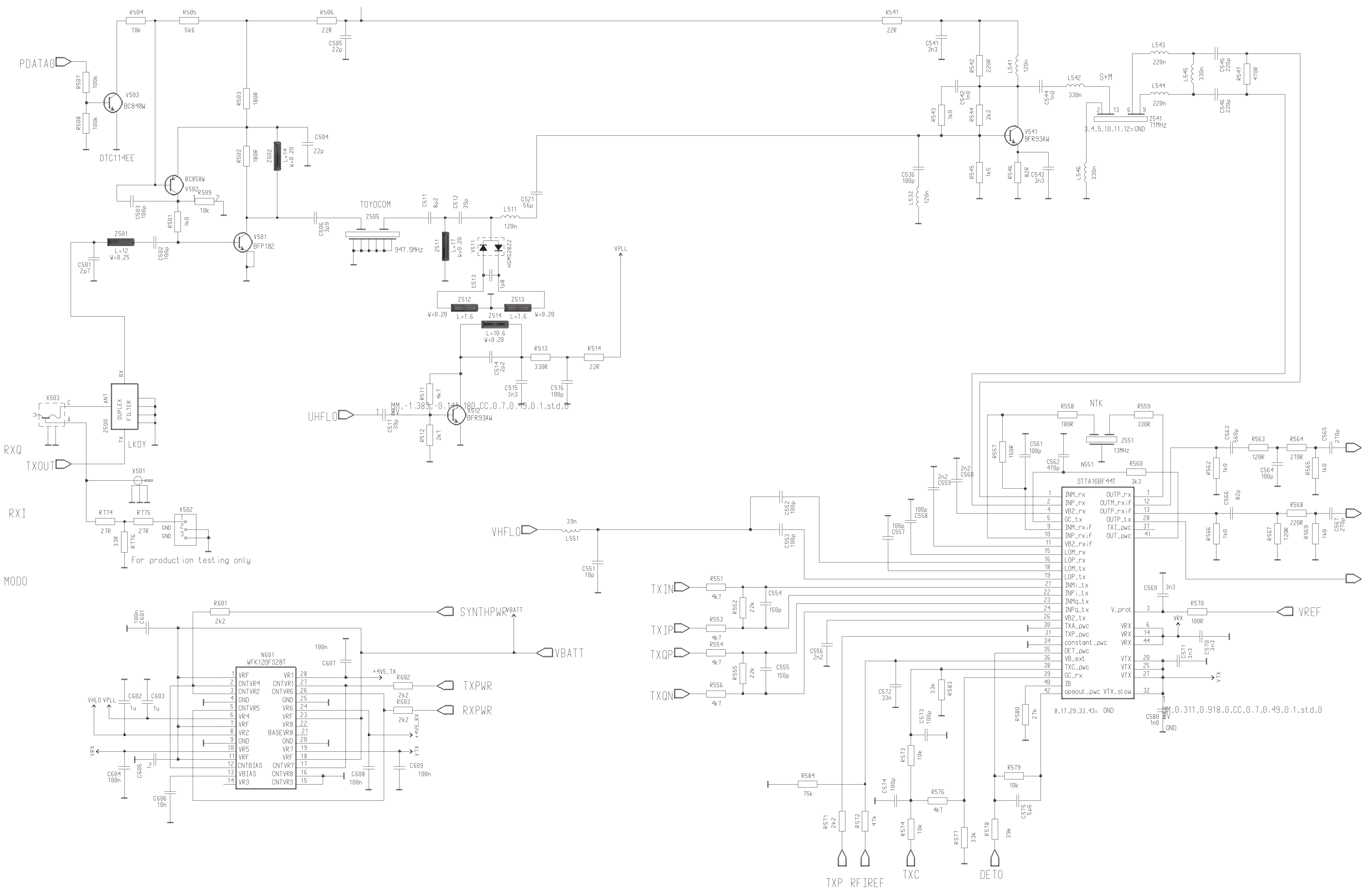


Figure 18   PCN Component Layout Bottom

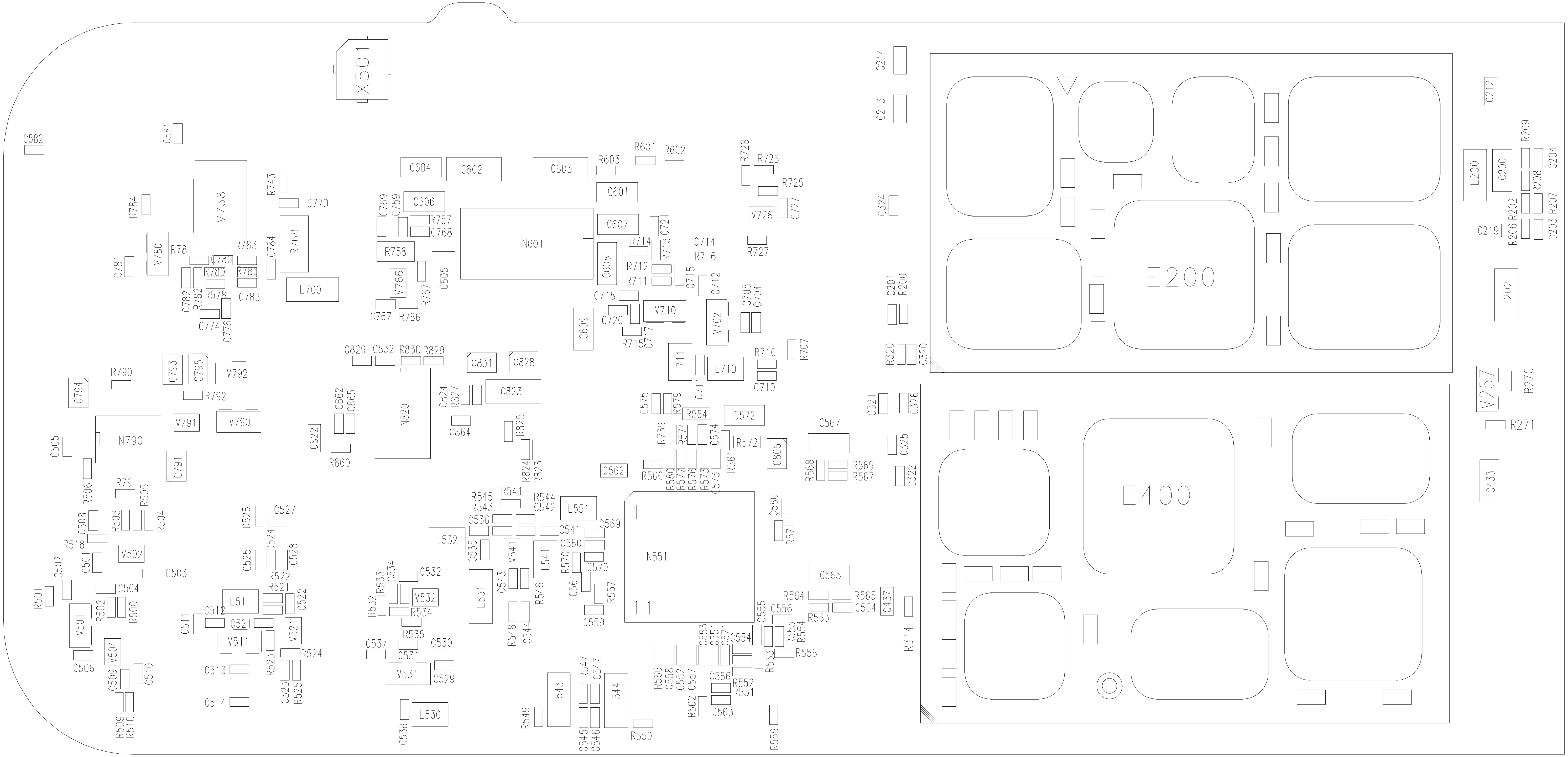


Figure 19 PCN Component Layout Top

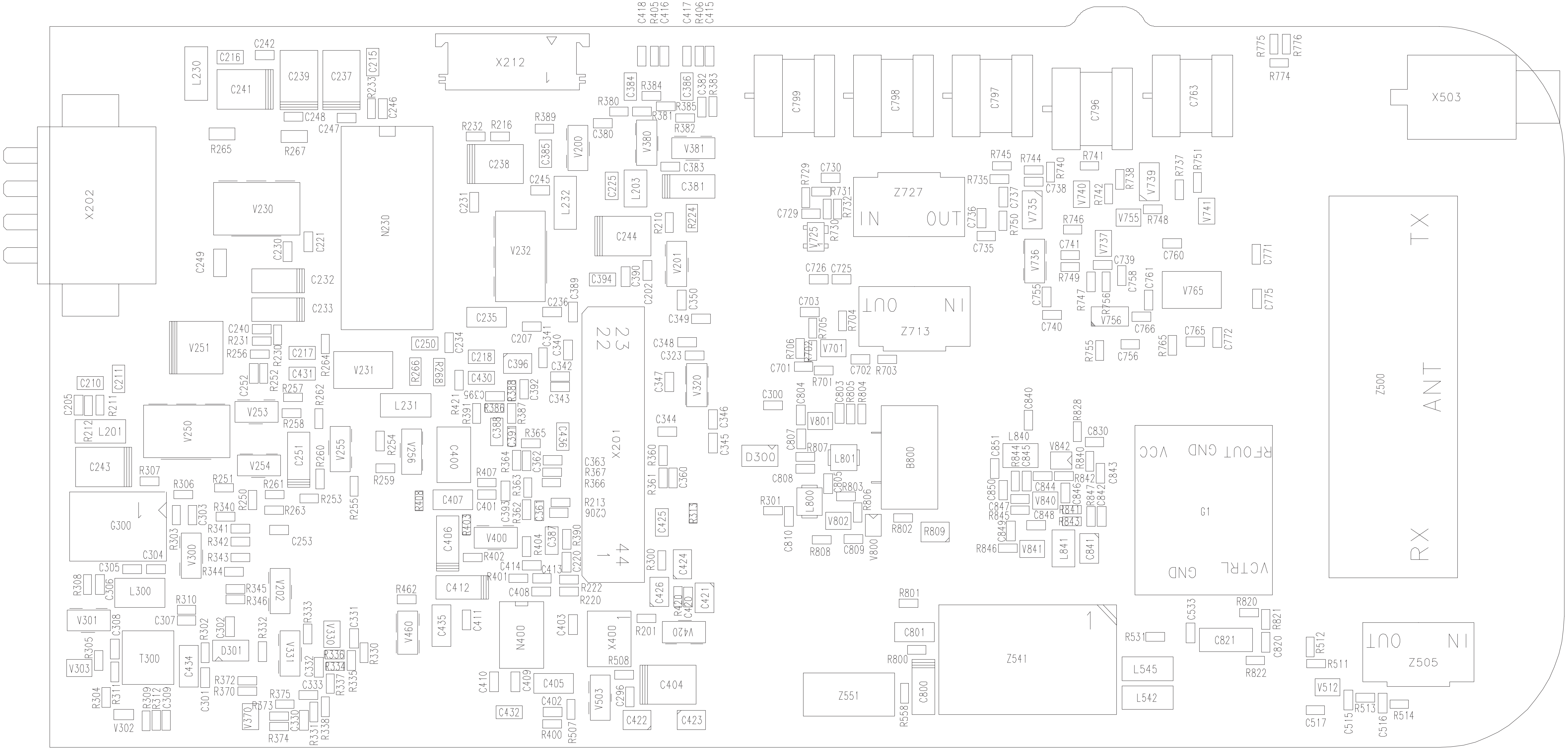


Figure 20 PCN RF / TX

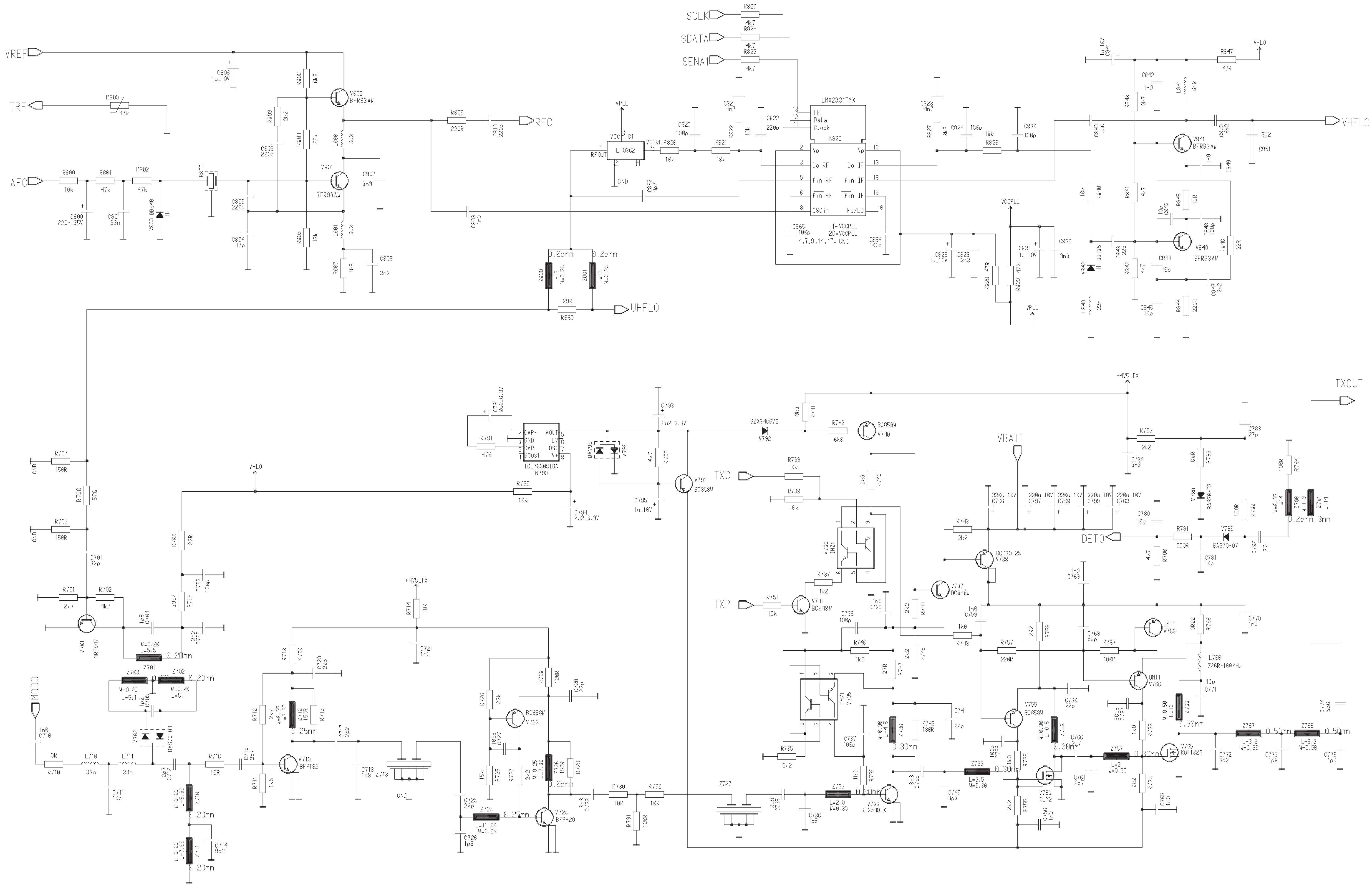


Figure 21 PCN RF / RX

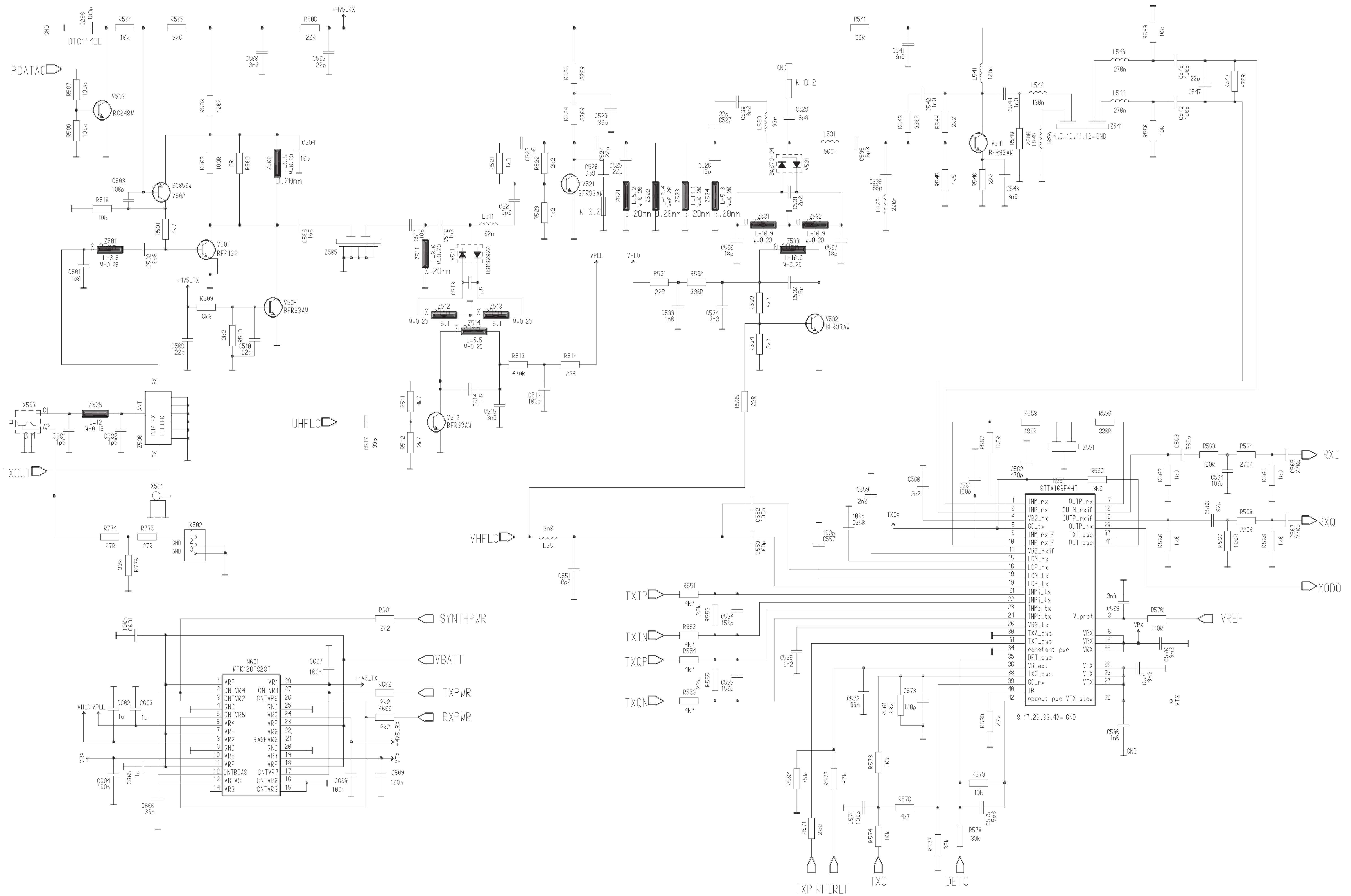


Figure 22 UIF Schematic – PCN

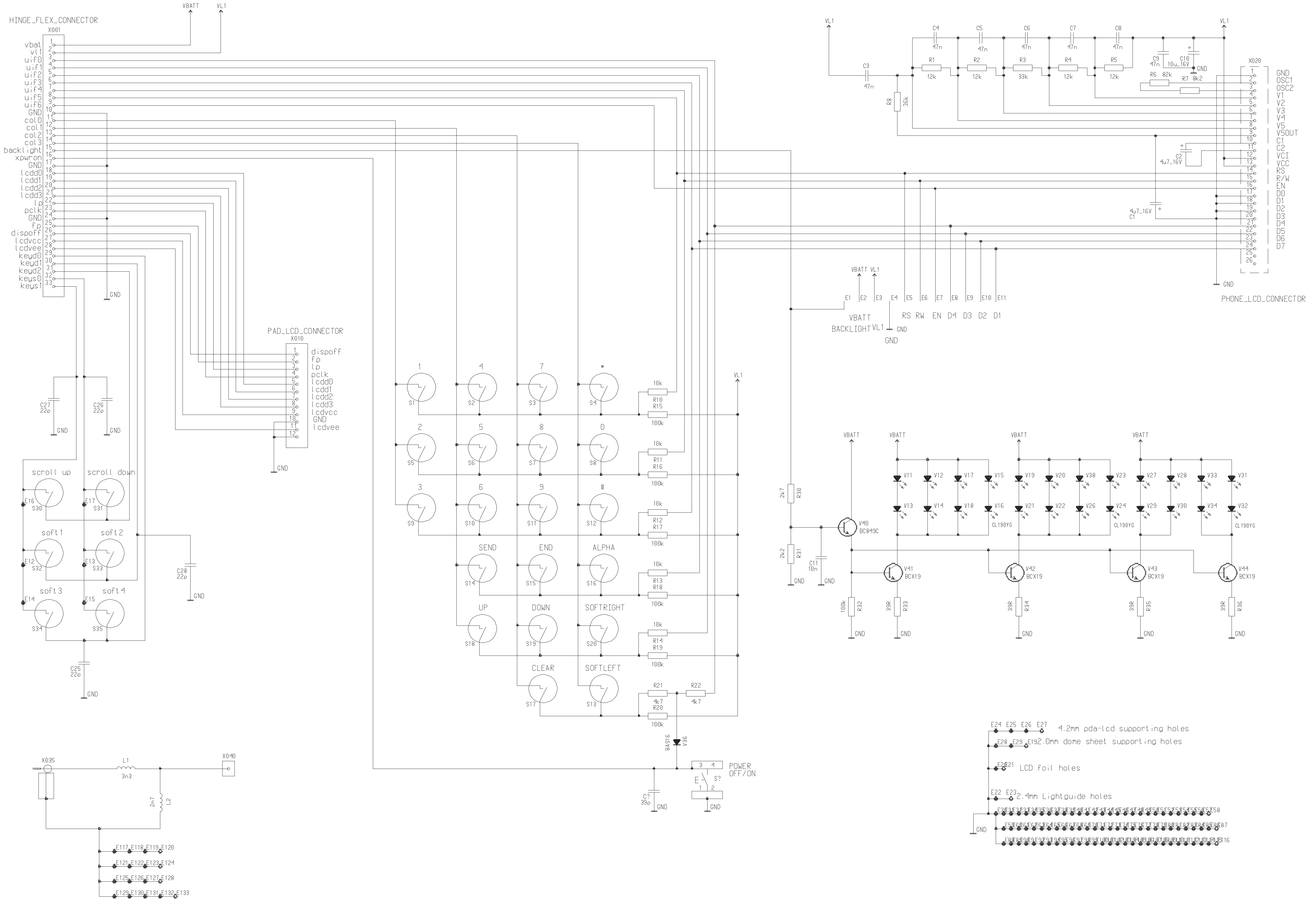


Figure 23 UIF Component Layout – PCN

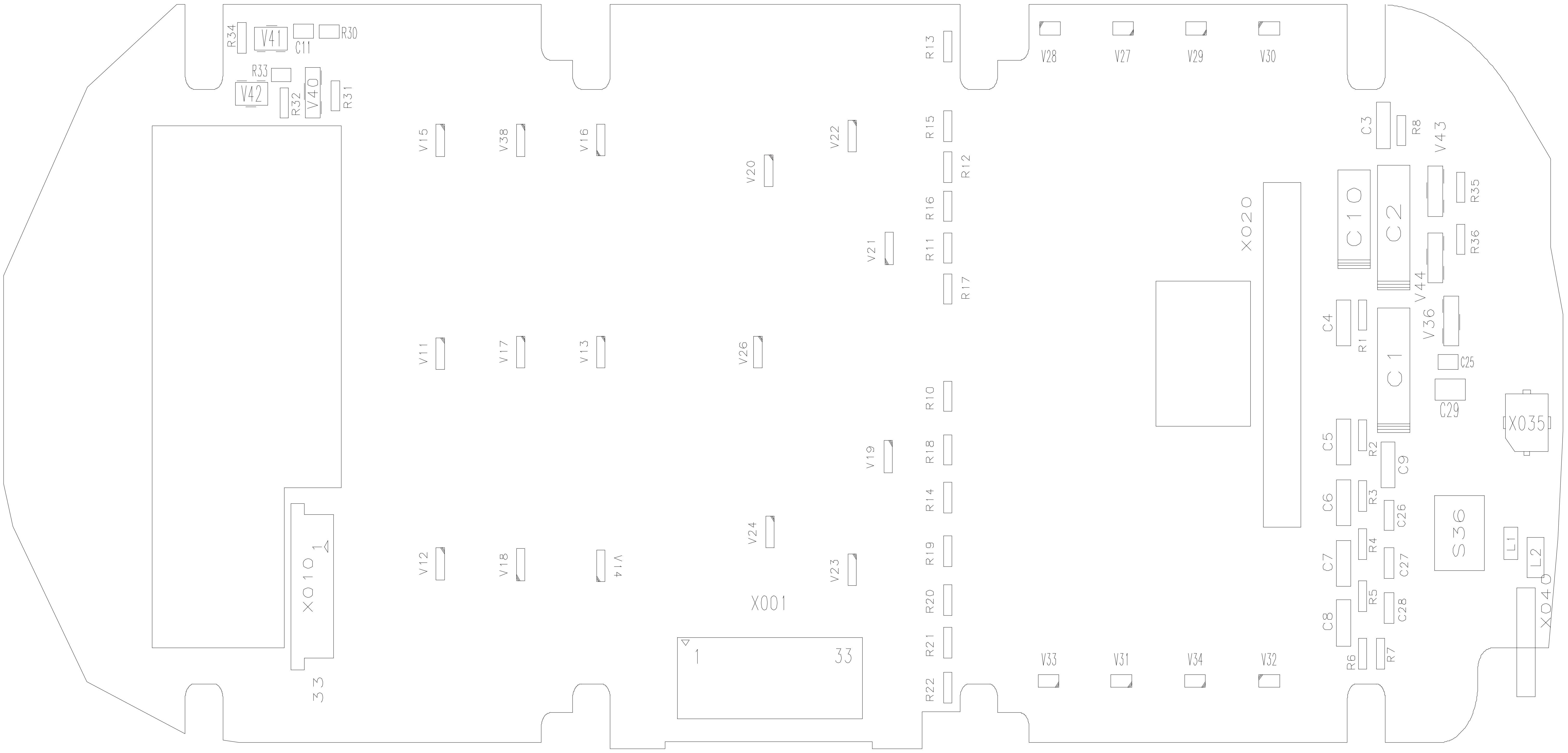


Figure 1 PDA Block Diagram
Edit 82 for layout 13a

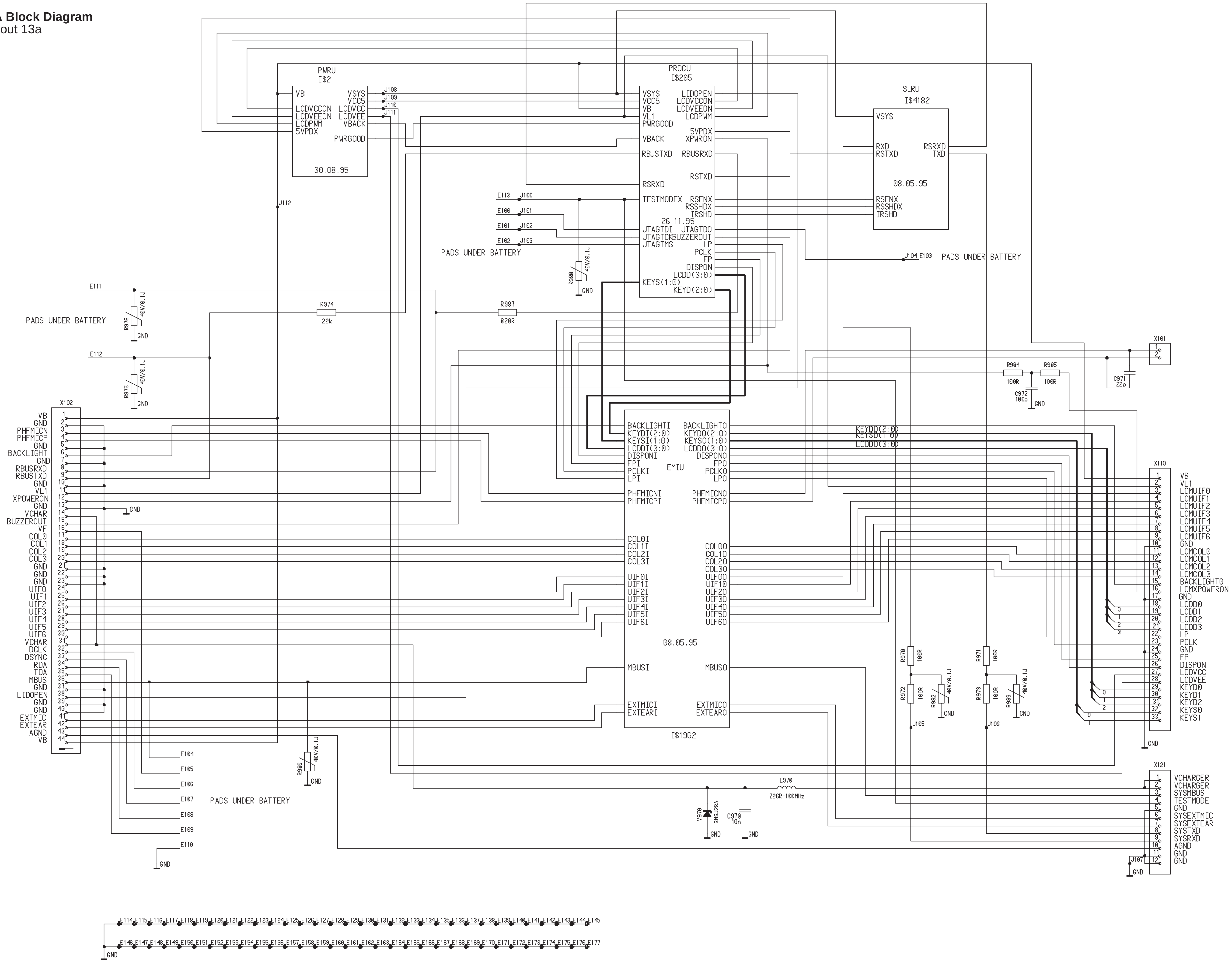


Figure 2 PDA Power Unit –PWRU
Edit 108 for layout 13a

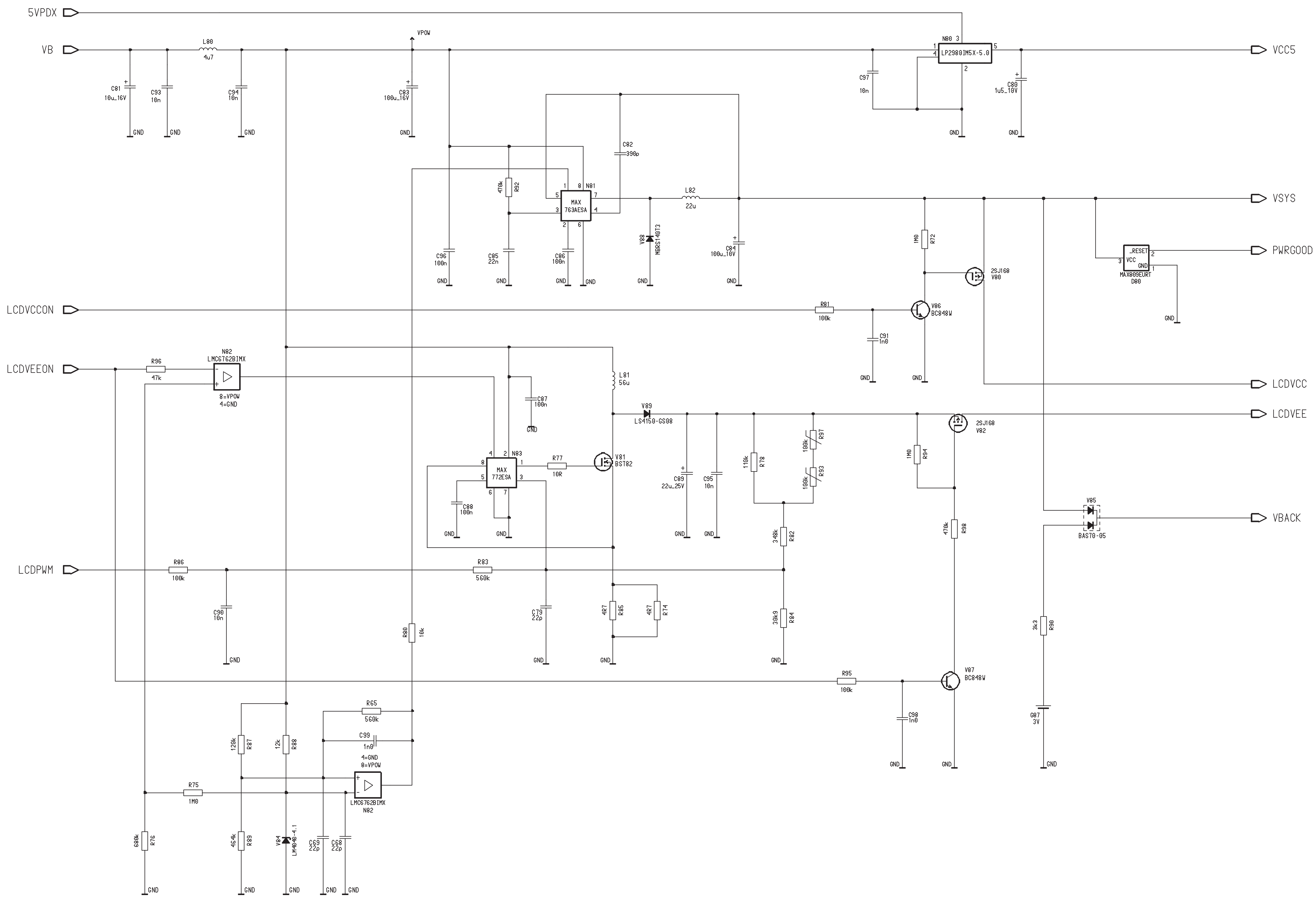


Figure 3 PDA Serial Interface – SIRU
Edit 24 for layout 13a

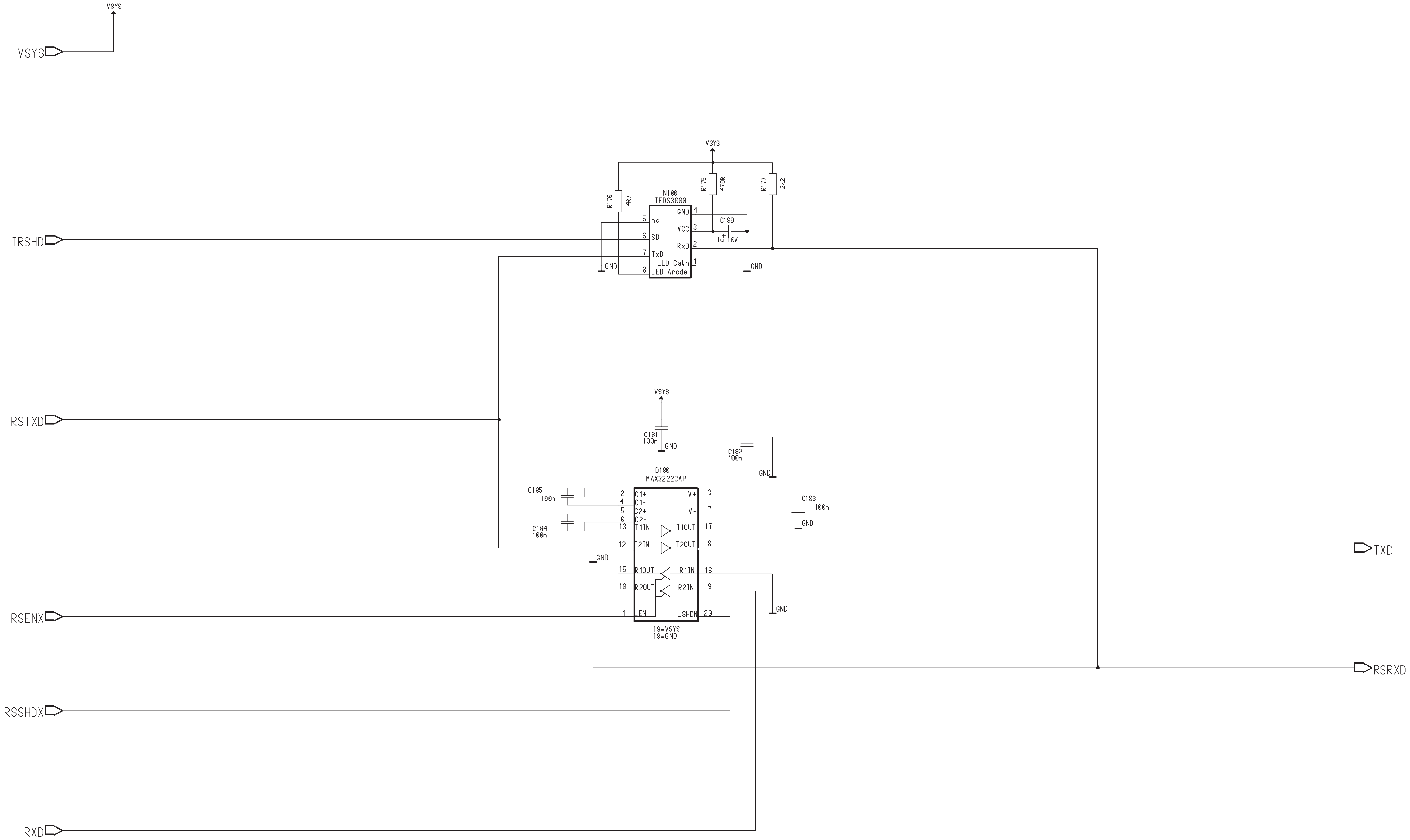


Figure 4 PDA MCU and Memory – PROCU
Edit 121 for layout 13a

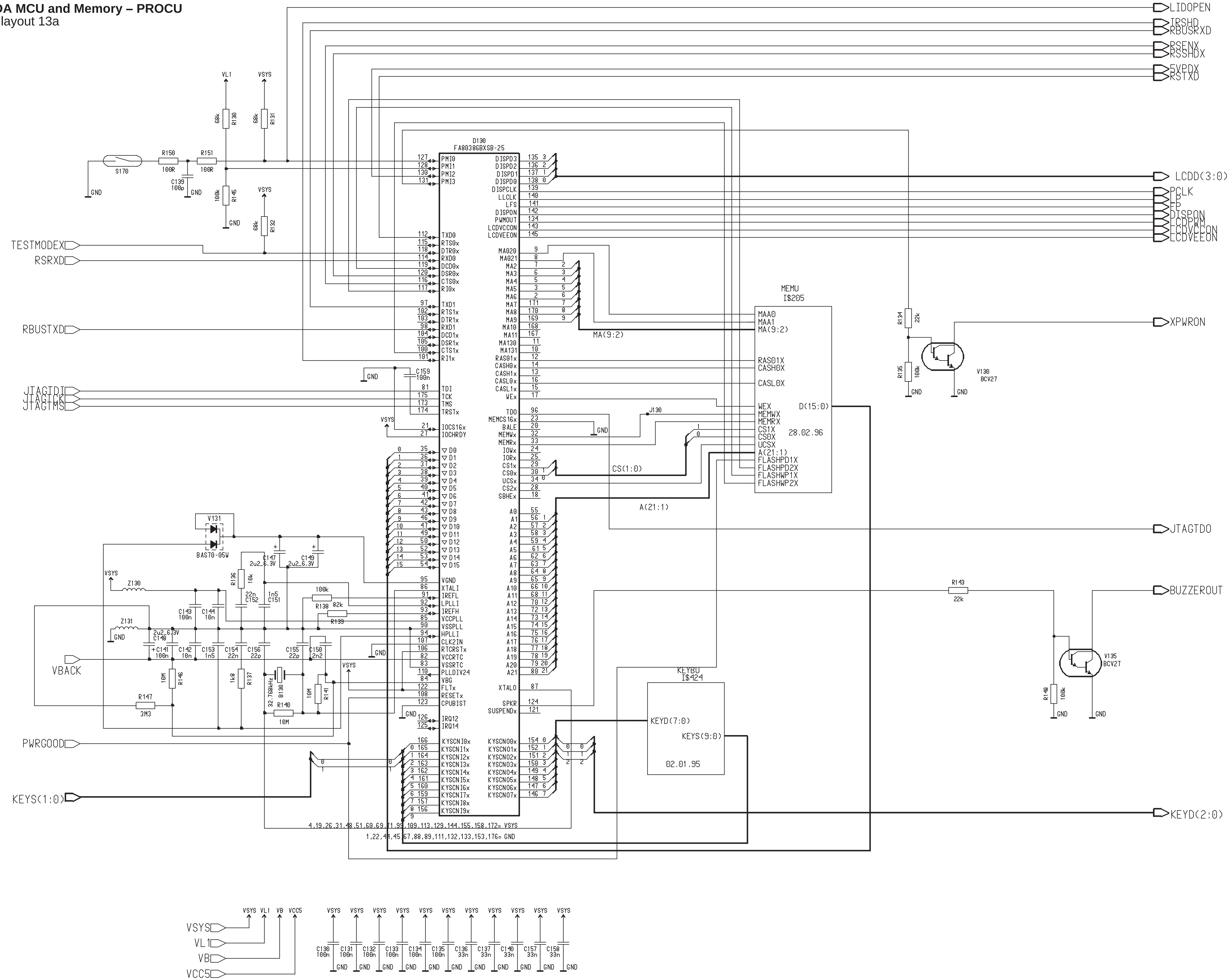


Figure 5 PDA EMIU
Edit 21 for layout 13a

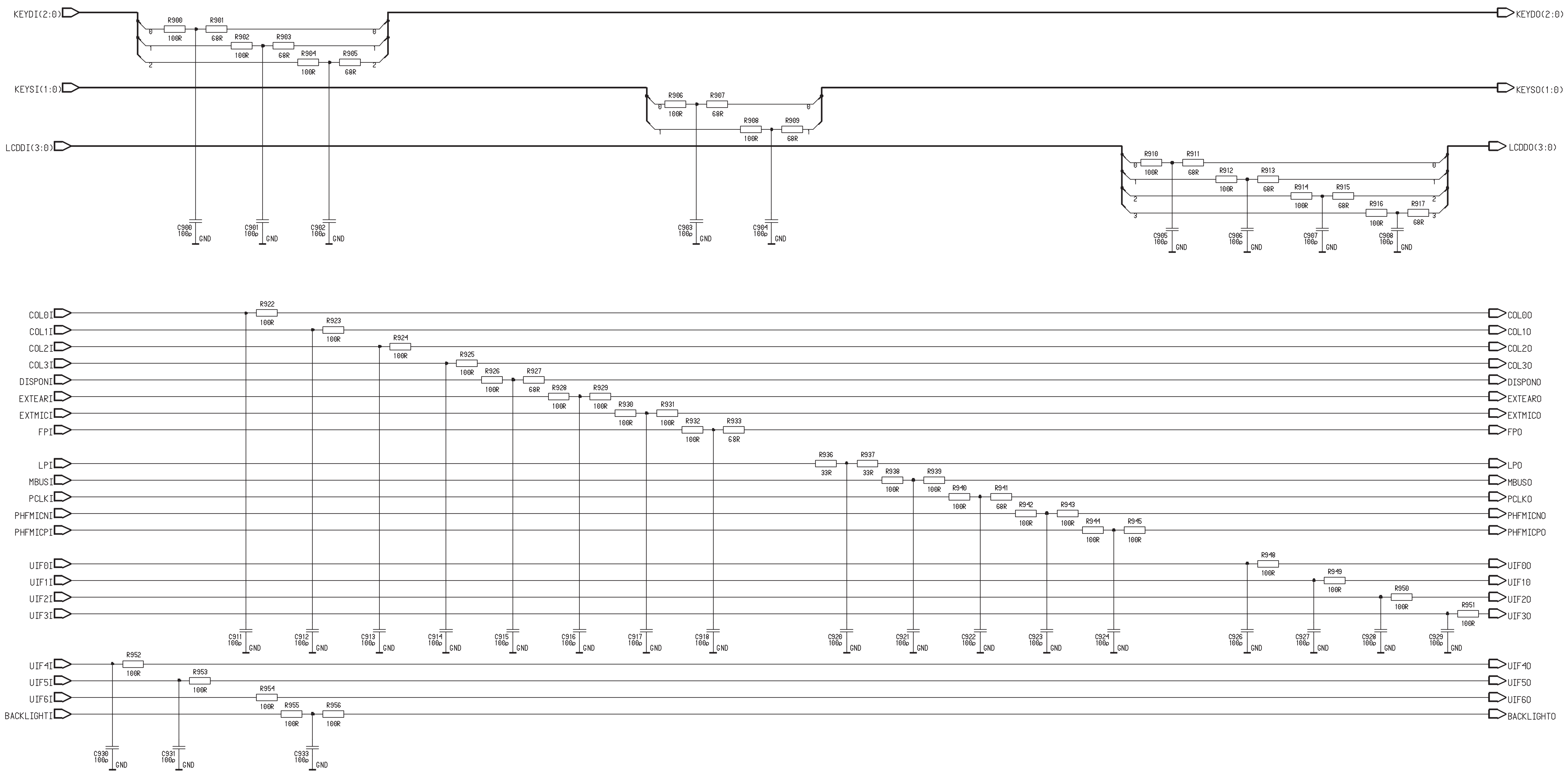


Figure 6 Keyboard matrix
Edit 24 for layout 13a

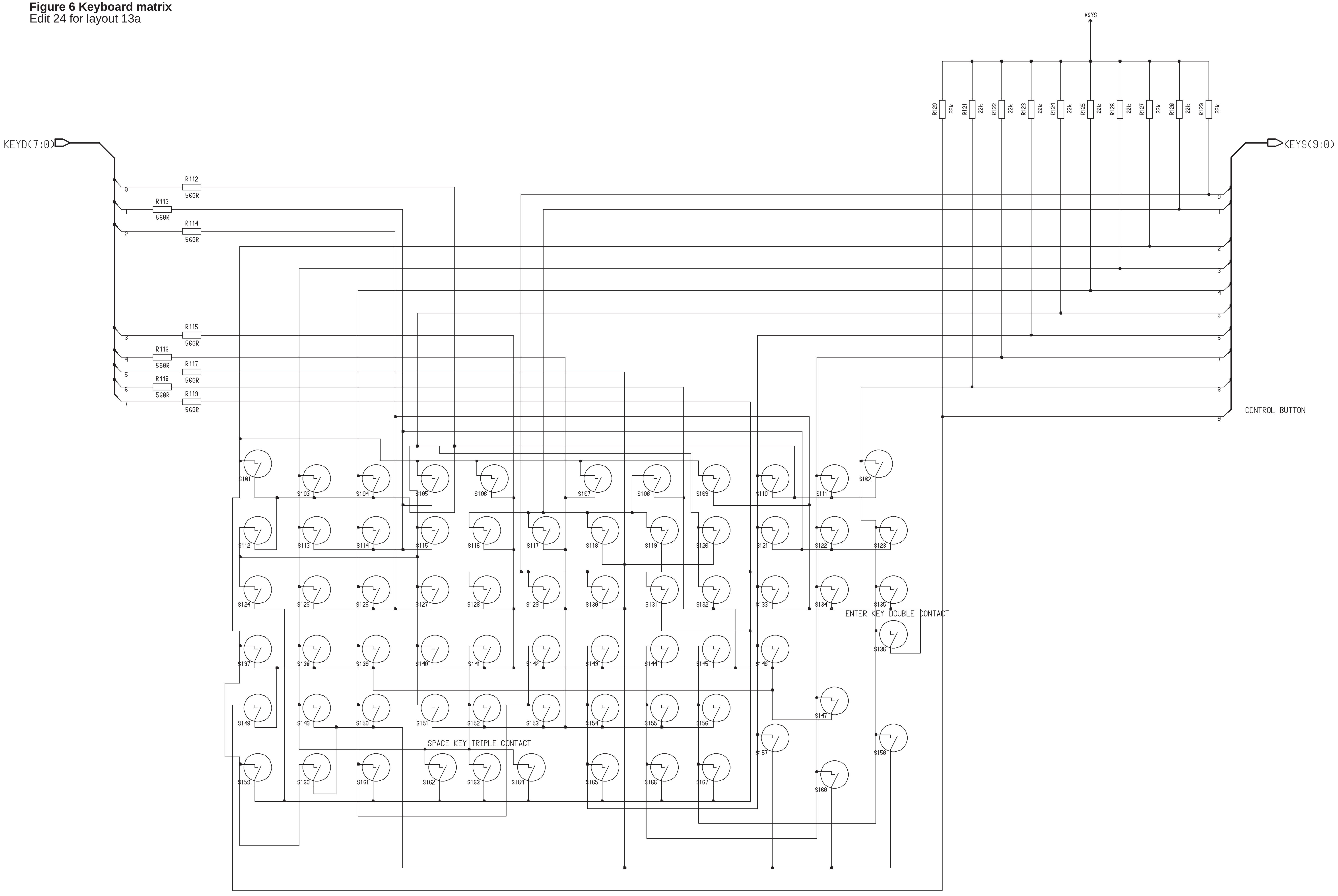


Figure 7 PDA Memory
Edit 28 for layout 13a

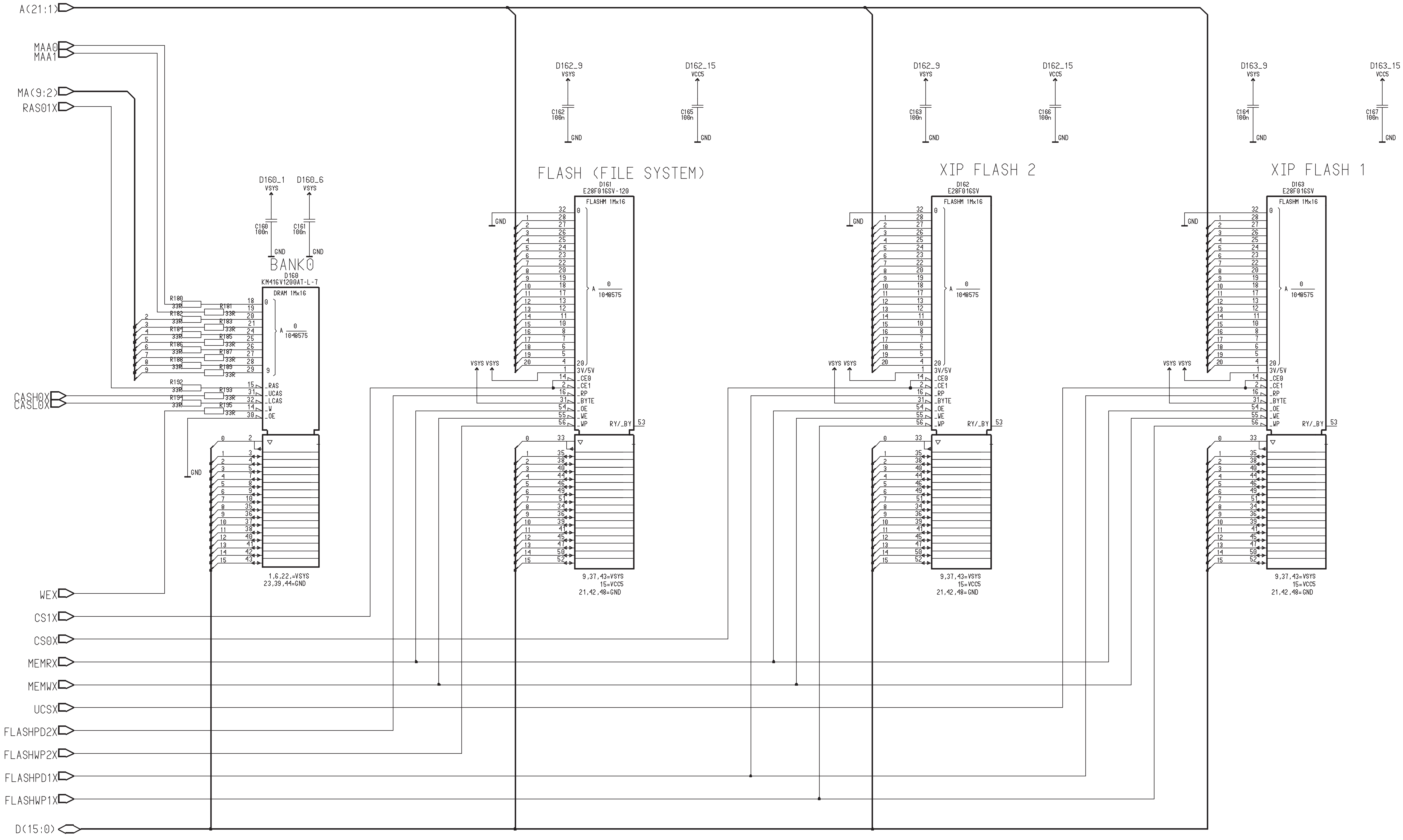


Figure 8 PDA Component Layout 13a

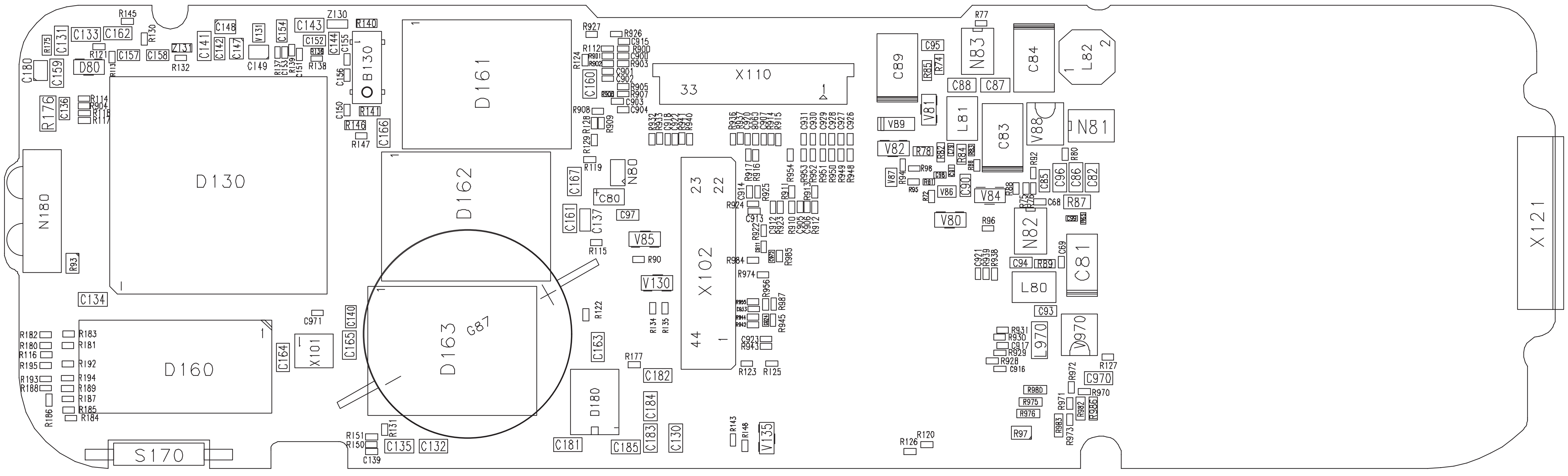


Figure 1. UIF Schematic

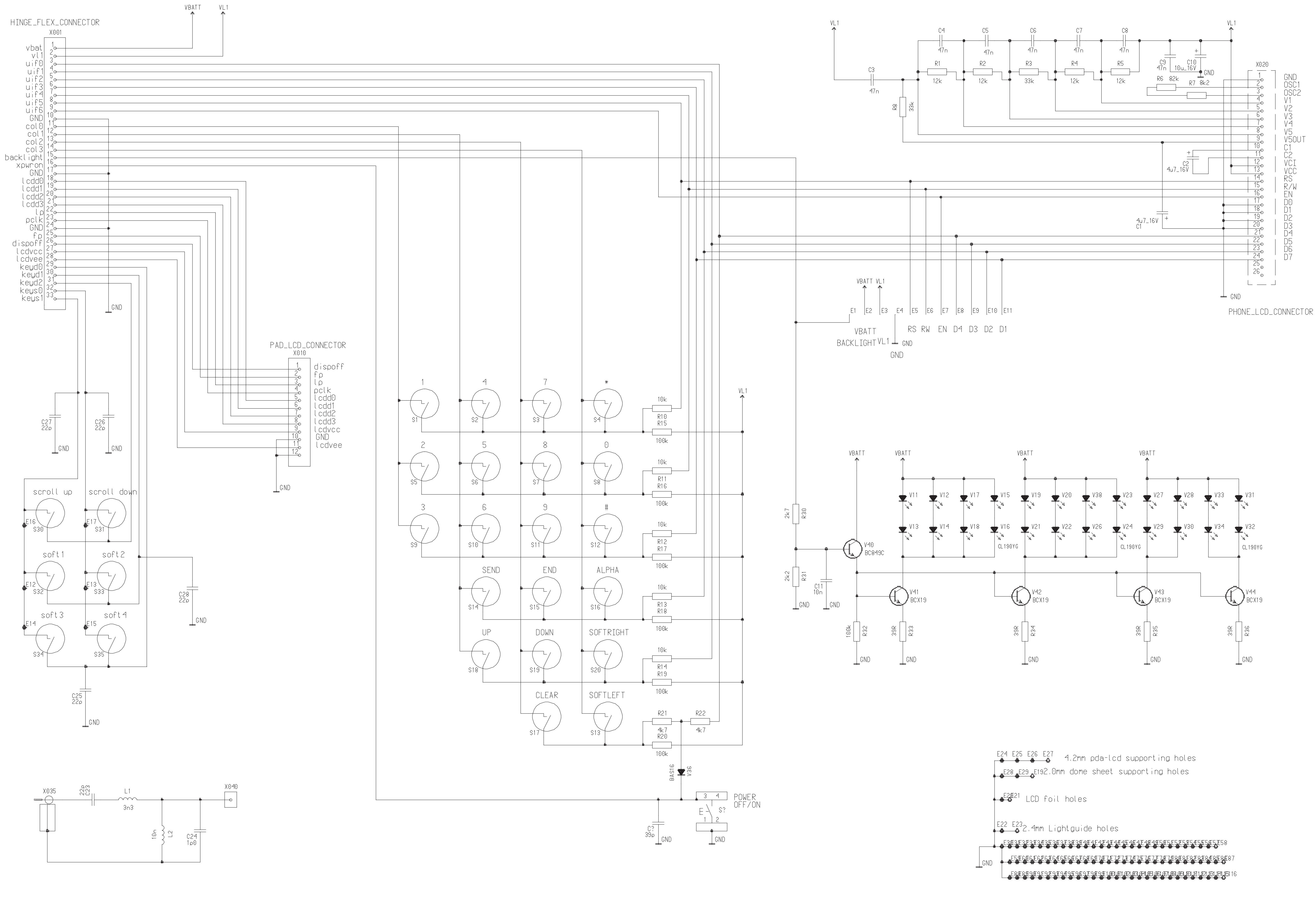
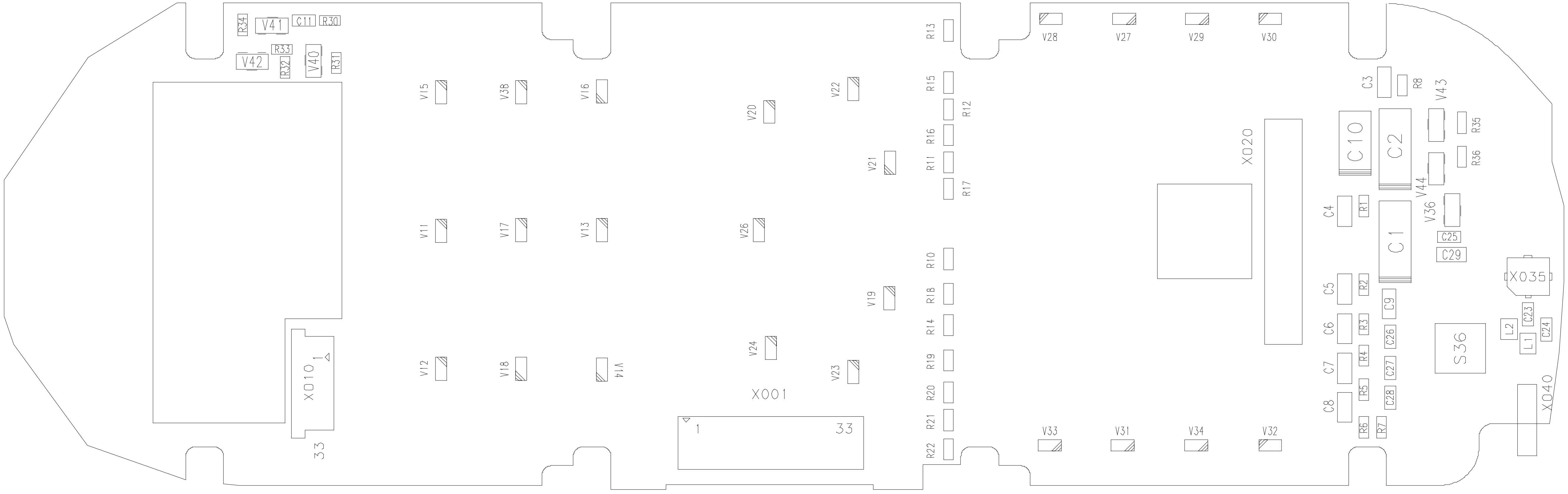


Figure 2 Component Layout – Uif



Accessories

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments

CONTENTS

List of Figures

Non–Serviceable Accessories

Battery Pack BLK–4S (0670153)

Purpose	a two cell Li Ion battery by SONY
Capacity	730 mAh
Battery connector	4 pin pad plate
Weight	82.5 $\pm$5 g
Charge time	2.5h
Charge voltage	8.4 $\pm$0.1 V
Charge current	800 mA
Volume	t.b.d.

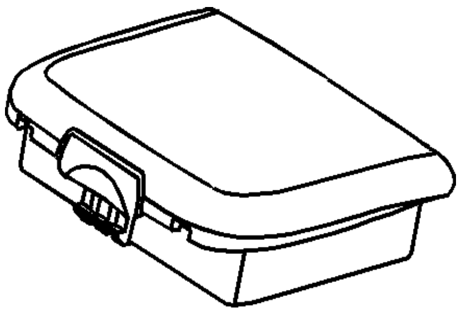


Figure 1. Battery pack BLK–4S

Universal Fast Charger ACH xxx

Purpose	fast charging of battery with transceiver
Charger type	switching mode power supply
Operation	constant current charging with limited voltage (12V nominal)
Input voltage	90–264 V 50 or 60 Hz
Mains plug type	Detachable AC cord to match any plug with local AC cord
DC connector	standard DC connector 3.8 mm
Weight	without AC cable 85 g, with AC cable 110 g
Volume	54 cm^3
Cable length	AC cable 200 mm; DC cable min. 300 mm, max. 2 m
Protection	output current limiting, max. 830 mA output voltage limiting, max. 13 V (unloaded)
Approvals	Specific for country where sold

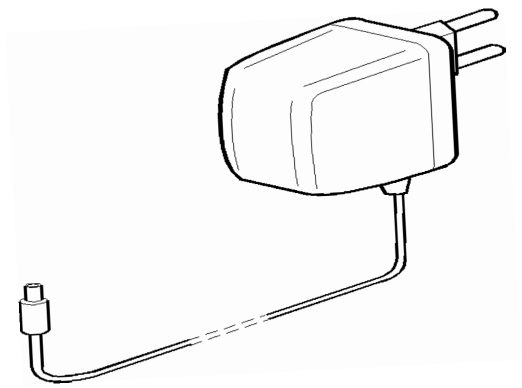


Figure 2. ACH type Fast Charger

Power Adapter Module PAR–1 (0680028)

Purpose	Connects ACP–3 and DLR–1 to RAE–1N system connector
DC connector	DC jack (thr. hole) for DC connector (3.8 mm) in ACP–3 (HEC2781–010010)
RS connector	Stereo jack for stereo plug (2.5 mm) in DLR–1 (HSJ2080–01–010)
Syst. con. socket	Pin probe (6 pin), thr. hole
Weight	8 g
Volume	10 cm^3

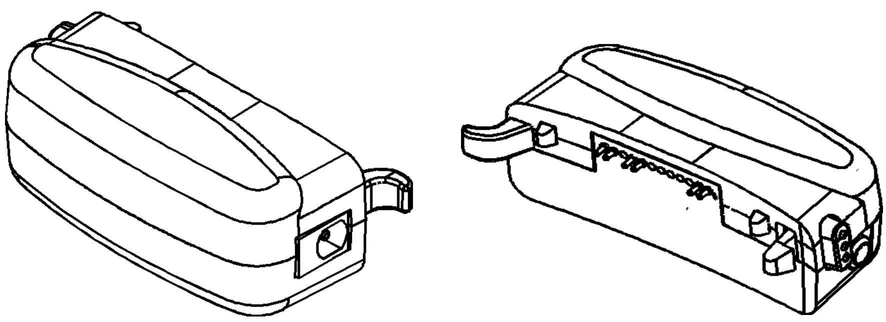


Figure 3. PAR–1: **left view**: ACP–3 connector; **right view**: System connector socket

RS232 Adapter Cable DLR–1 (073077)

Purpose	Connects an external computer with RAE–1N (via PAR–1) see below
Cable length	950mm ± 25 mm (3 wire, ⌀3.5 mm)
D connector	D9 connector female
Stereo connector	Stereo plug (⌀2.5 mm) with ⌀3.5 mm strain relief

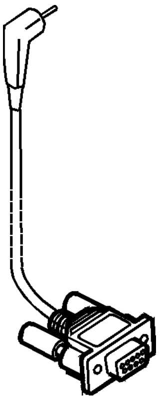


Figure 4. DLR–1

Connection

The connection of DLR–1 cable is shown below. The signals are routed directly from end to end of the cable. The shield of the cable is connected only in the PC connector side, directly to the shield pin of the D–connector.

The connection to the communicator side is soldered.

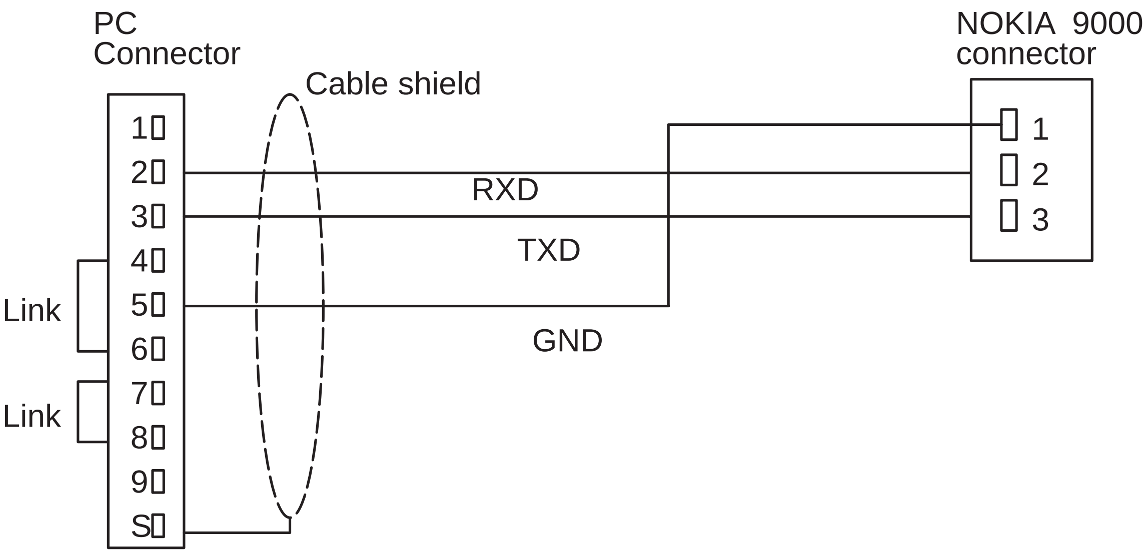


Figure 5. Circuit diagram of DLR–1 cable

Cigarette Lighter Charger LCH–2 (0675005)

Purpose	charging adapter for car environment; input voltage 9...32 V
Charger type	Switching mode power supply
Operation	quick charge (< 0.5–2.5 h), trickle charge
Protection	input fused, output current limit
Connectors	output: 3.8 mm standard DC plug; input: D 21 / 23 mm
Weight	<120 g
Cable	2 m curly cable

NOTE! The current version of LCH–2 does not indicate (led illumination) in a correct way what is the status of the charging with Li batteries.

For quick car installation, the user can utilise the Cigarette Lighter Charger LCH–2, Power Adapter PAR–1, and RS232 serial cable DLR–1 Mobile

Holder MBR–1 cannot be used in this context.

Serviceable Accessories

Spare Battery Charger DCH–4 (0675107)

Purpose	BLK–4S stand alone charger for spare batteries
Charger type	Linear mode power supply
Operation	quick charge (2.5 h)
DC connector	DC jack (thr. hole) for DC connector (3.8 mm) in ACP–3 (HEC2781–010010)
Battery connector	4 pin spring
Oper. input voltage	12 Vdc ±1V
Weight	61 g
Input current	800 mA ± 80 mA
Charging temp.	0–45 °C

The DCH–4 Desktop Charger is designed for standalone charging of a spare battery, which is only the Lithium type specified for the phone. There is no battery type detection in the desktop charger. In a standard configuration, rapid charging is possible by connecting the desktop charger to an ac power outlet via a suitable constant current ac adapter (ACH–4, ACP–3). This is connected to the dc connector, X130.

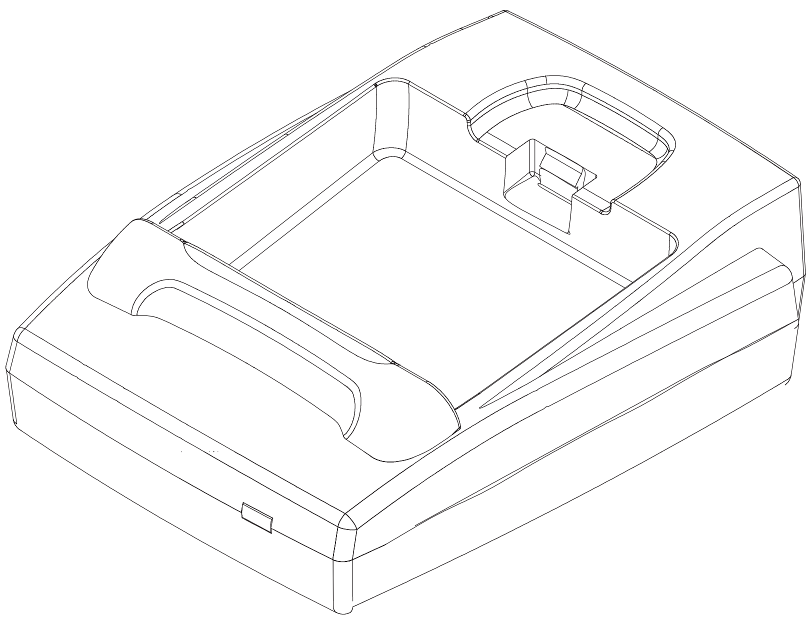


Figure 6. Spare battery Charger DCH–4

Operation

The device has a dc plug input connector for the ACP–3 charger and 4–pin output connector for an extra battery. Recommended charging temperature is between 0 ... 45 degrees centigrade. Charge control of the spare battery is done with a constant voltage controller and dissipative transistor located in a desktop charger PCB.

Charging indication

Charge is indicated with two LEDs, red and green. They both shed their light into same mechanical light guide.
Red LED indicates that the battery is not full. This color is shown to user until current to battery decreases under 65mA.
Green LED indicates that the battery is full but charging of the Lithium battery continues after green indication to ensure the maximum capacity. Charging is stopped completely after current to battery decreases below 30mA. Green LED stays visible until battery or charger is removed.

When battery is disconnected and charger is connected, LEDs are off. When charger is disconnected and battery is connected, LEDs are off. Battery is not discharged so there is no harm in leaving the battery to desktop charger for long periods. For example during trips it is a benefit to carry both spare battery and desktop charger together in small space. When full battery is reconnected to desktop charger, LED color is first red and after couple of seconds it turns green. Red color is shown because charge is started again and correct indication is given only after measured current value settles down.

Charge Control

Charge current for the battery is supplied through a series pass transistor in desktop charger. This transistor is fully on when voltage of the battery is under maximum value: 8.4V or 8.2V, depending on battery chemistry. During this condition charger is supplying a constant current to the battery. After voltage rises to maximum value, pass transistor controller IC: N115 limits the voltage so that current to battery begins to decrease. This is the same action as in linear regulators.

Energy equal to voltage difference over pass transistor times current through it transforms to heat. This requires big PCB area to dissipate the heat. Current begins to fall rapidly after highest battery voltage is reached so heat load comes in intensive transient. Large copper area in PCB is required to absorb the peak heat energy. Some energy losses are also transformed to heat in diode and current measuring resistor after pass transistor.

Battery voltage feedback to controller is taken from battery terminal so that there is no voltage drops of series elements. Current to battery is measured by instrumentation amplifier which outputs absolute voltage proportional to voltage difference of its inputs.

Small resistor R112 is put to make this little voltage difference in main current path. Voltage gain over R112 is 83 in the amplifier. This is compared to two reference voltages. First determines the current at which LED color is changed: 65mA. Second reference is put for stopping the charge at lower current value: 30mA. This is made to ensure that there is no capacity loss in Li–Ion battery if it remains in desktop charger many days.

Different Charging Voltages

Two cell Lithium–Ion carbon technology requires 8.4V constant voltage charging. Two cell Lithium–Ion graphite technology must be charged by 8.2V constant voltage. Because the controller is already set to 8.4V charging, higher voltage reference and voltage dividor from reference to battery voltage is required to feed 8.4V to controller and maintain 8.2V in battery line for graphite batteries. Because the reference is zener, its voltage is not stable unless current is set high enough. Voltage tolerance of charger sets minimum current value at this voltage: 10V. Nominal charger voltage makes zener current high. This also makes high leakage current path from battery to regulator input. V148 is cutting this current path when either charger or battery is disconnected. Battery chemistry is detected by battery type sense resistor which is connected to ground inside battery pack. Connecting battery biases pin 5 of N110 so that either voltage is selected when charging starts. V147 controls the voltage shown to charge controller N115. If V147 conducts battery voltage is directly fed to controller resulting 8.4V charging. If V147 is off, voltage dividor makes battery voltage 8.2V.

DC Characteristics

Table 1. Battery type sense resistor values inside battery pack

Notes	Typical / Nominal
Operating input voltage:	12 Vdc ±1V
Max. input current:	800 mA ±70 mA
Charge voltage (type sense resistor: 100k)	8.4 V
Charge voltage (type sense resistor: 68k)	8.2 V
Typical power consumption	10 mA

Table 2. Supply Voltages and Power Consumption

Notes	Typical / Nominal
Operating input voltage:	12 Vdc ±1V
Max. input current:	800mA ±70mA

External Signals and Connections

Table 3. List of connectors

Connector Name	Code	Notes
Fast charger ac adapter connector	X130	2–pole DC–jack
Spare battery connector	X120	To the flex cable of 4–pin spare battery.

Table 4. Fast charger ac adapter connector X130

Signal Name	Pin / Conn.	Notes
VDC	1	supply voltage input
GND	2	common ground
–	3	mechanical support pin, connected to ground

Table 5. Spare battery connector

Signal Name	Pin / Conn.	Pin / Conn. Outlook contacts	Notes
VBAT	X153	1	battery positive terminal
BTYPE	X152	2	battery type sensing terminal
SPARE PIN	X151	3	not connected
GND	X150	4	common ground

Outlook contacts are referred so that 1 is nearest to edge of desktop charger and 4 is most inner pin.

Mechanical Characteristics

Unit	Dimensions (mm) (W x L x H)	Weight (g)	Enclosure (material etc.), colour
DCH–4	71.0 x 91.5 x 27.0	56	Material: ABS / PC Color: Warm black
PCB	63.9 x 83.6 x 1.0		
DC jack X130 for ACH–4	3.8 x 1.3, centre contact positive		

Environmental Conditions

Table 6. Allowed Ambient Temperature (charging)

Environmetal parameter	Unit	Use
Low air temperature	°C	+ 0
High air temperature	°C	+45

Table 7. Allowed Ambient Temperature (transportation and storage)

Environmetal parameter	Unit	Use
Low air temperature	°C	–40
High air temperature in unventilated enclosures 1)	°C	+85
High air temperature in ventilated enclosures or outdoor air	°C	+40

Assembly

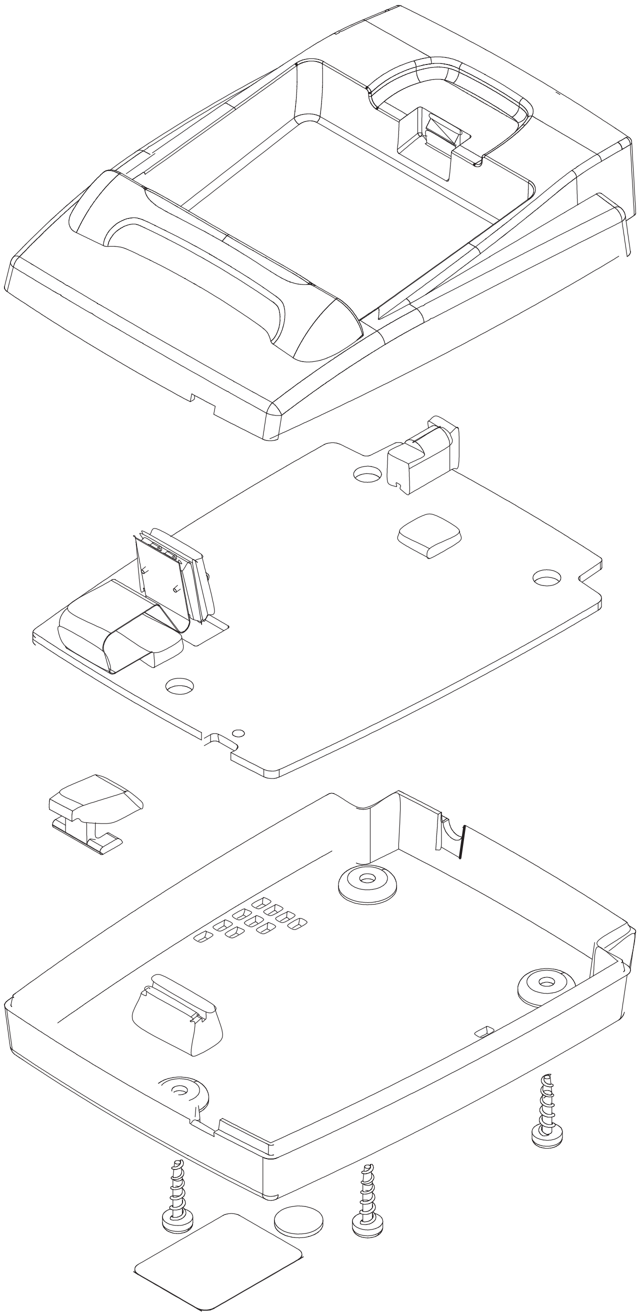
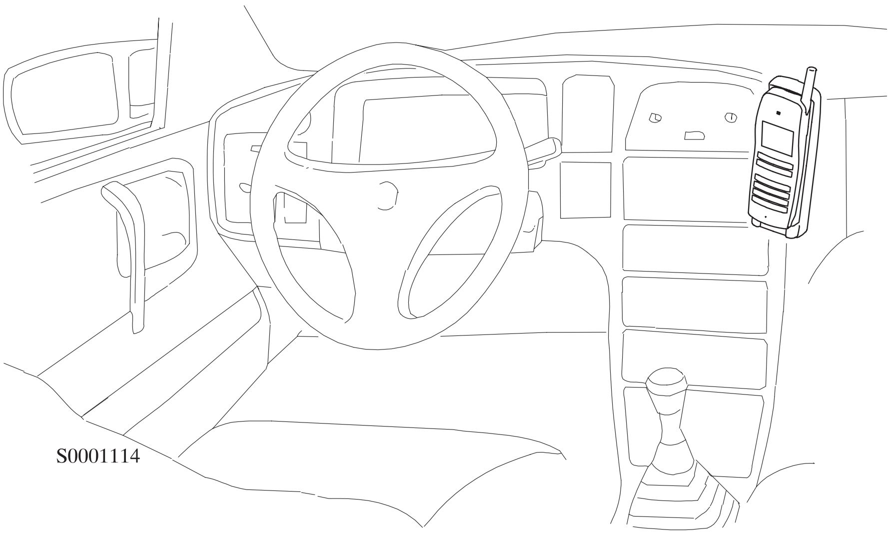


Figure 7. Exploded view DCH–4

CARK60 Hands–Free Car Kit (0086052)

Information on this package is covered in the Vehicle Installation Guide P.N 0275190. This is a similar document ,adapted for the service manual, to the one included with the actual sales package

CARK60 Installation Guide



Original, 08/96

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments

CARK60 INSTALLATION GUIDE

CONTENTS

List of Figures

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Introduction

This installation guide has been prepared to provide the basic information necessary to install this car kit. This guide is not intended to be definitive, because different types and models of vehicles will require different installation work. The information given is for general guidance only.

The terms of warranty demand that this car kit be installed by an experienced installer and only genuine Nokia parts be used. An end user should never attempt to install this car kit without professional assistance as the installation requires special tools and knowledge.

Please refer to the NOKIA 9000 communicator's User's Manual and Accessory Guide for instructions on the telephone's operation, care and maintenance, including important safety information.

Note: Read the warnings below before beginning the installation procedure.

WARNINGS

ENSURE THAT THE VEHICLE'S BATTERY IS DISCONNECTED BEFORE YOU START THE INSTALLATION PROCEDURE, AND THAT IT REMAINS DISCONNECTED DURING THE PROCEDURE.

DO NOT SMOKE OR USE OPEN FLAMES WHEN WORKING NEAR THE VEHICLE'S FUEL SYSTEM.

ENSURE THAT ELECTRICAL CABLES, HYDRAULIC LINES AND FUEL LINES ARE NOT DAMAGED DURING INSTALLATION.

ENSURE THAT NORMAL CONTROL AND OPERATION OF THE VEHICLE IS NOT IMPAIRED BY THE INSTALLATION, PARTICULARLY THE BRAKES AND STEERING.

ALTHOUGH ELECTRONIC SPEED CONTROL, ABS ANTI–LOCK BRAKE AND FUEL INJECTION SYSTEMS ARE RELATIVELY IMMUNE TO MALFUNCTION CAUSED BY NEARBY RADIO TRANSMISSIONS, SHOULD YOU EXPERIENCE FALSE OPERATION OF THESE SYSTEMS OR ARE IN ANY DOUBT WHATSOEVER AS TO THEIR FUNCTIONALITY, PLEASE CONSULT THE VEHICLE'S DEALER.

THE CAR KIT IS SUITABLE FOR USE ONLY IN VEHICLES WITH A 11..32 V NEGATIVE GROUNDING. USE ON OTHER SUPPLY VOLTAGES OR ALTERNATIVE POLARITY WILL DAMAGE THE EQUIPMENT.

THE PHONE SHOULD NOT BE LEFT SWITCHED ON FOR EXTENDED PERIODS WITHOUT RUNNING THE VEHICLE'S ENGINE. FAILURE TO COMPLY COULD DRAIN THE VEHICLE'S BATTERY.

Unpacking

Carefully unpack the equipment and ensure that the following items are present.

Charging Holder	MBR–1
Junction Box	(to be mounted with MKE–1) HFJ–3
Mounting Plate	(w/12 screws, 4 nuts, 4 washers) MKE–1
Swivel Mounting Plate	(incl. mounting plates & screws) MKR–1
Flat Mouning Kit	(incl. mounting plates & screws) MKK–1
Hands–Free Microphone	HFM–10
Hands–Free Speaker	(w/2 screws) HFS–6
Power Cable	(w/2 fused connectors & wire ends) PCH–4

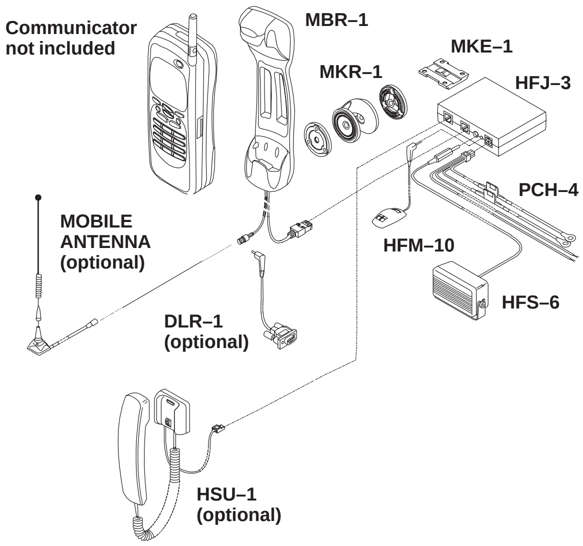

Figure 1. CARK60 Kit and options

Component Parts

Charging Holder MBR–1

The Charging Holder unit offers your Communicator an external antenna connection, hands–free function, and firm attachment to the vehicle. The installation of the Holder can be done in two different ways: either 1) using Swivel (adjustable angles) or 2) using Flat Mounting Kit (fixed position).

Mounting Plate MKE–1, Flat Mounting Kit MKK–1 and Swivel MKR–1

The Mounting Plate is used to mount the Hands–Free Junction Box. Screw the Mounting Plate to the appropriate place and slide on to the Junction Box.

RAE / RAK–1N Series

The Swivel or the Flat Mounting Kit can be used to mount the Holder to the vehicle. The Swivel is for adjustable mounting angles for each end of the Holder and the Flat Mounting Kit is for mounting in a flat, fixed position.

To install the Holder using the Flat Mounting Kit:

1) Attach the Snap Mounting Plate to convenient location using the four black screws provided.

2) Attach the Fixed Mounting Plate to the Holder (at whichever end is suitable) using the three silver screws provided.

3) Attach the Adapter Plate to the Fixed Mounting Plate using one of the large mushroom–head screws.

4) Slide the Adapter Plate on to the Snap Mounting Plate.

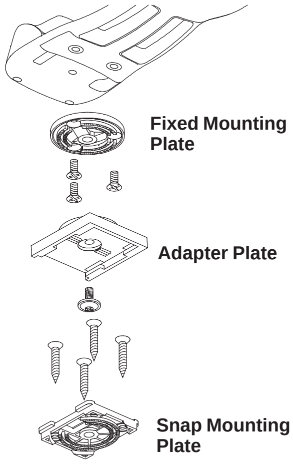

Figure 2.   Flat Mounted Fixing Kit

To install the Holder using the Swivel:

1) Attach one of the Fixed Mounting Plates to a convenient location inside the vehicle using the three black screws. Attach the other Fixed Mounting Plate to the Holder (at whichever end is suitable) using the three silver screws.

2) Fasten a Swivel Body to the Fixed Mounting Plate on the Holder using one of the large mushroom–head screws. Before tightening the screw, ensure that the Swivel Body is oriented to suit the mounting location. Repeat this procedure for the Swivel Body which is to be attached to the Fixed Mounting Plate on the vehicle.

3) Position the Holder in the desired orientation so that the teeth of the Swivel bodies interlock. Fasten the bodies together using the silver bolt and nut.

4) Once the desired position has been obtained ensure that all the screws are fastened securely.

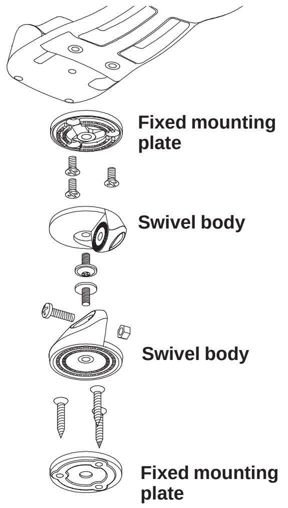

Figure 3. Swivel Mounted Fixing Kit

Junction Box HFJ–3

The Hands–Free Junction Box provides and controls the supply voltages for the accessories and charging current for your Communicator. In addition, it controls the audio paths to accessories and hands–free equipment. The jack marked HANDSET/ACCESSORY is reserved for the optional handset.

Hands–Free Microphone HFM–10 and Speaker HFS–6

The Hands–Free Microphone connects directly to the Junction Box MIC jack and Hands–Free Speaker to the SPEAKER jack.

Power Cable PCH–4

The Power Cable connects to the Junction Box via the 4 pin connector. The red (+12 V) and black (GND) wires connect to the battery via the supplied fused connectors. The yellow (XCRM) wire is for car radio mute and the blue (IGNS) wire is for ignition sense. The XCRM line goes down to 0 volts during a call. The maximum sink current is 250 mA (see “Installation; Car Radio Muting”). The IGNS line is connected to a +12 V voltage source, controlled by the Car Ignition Key. The Ignition Sense can utilize voltages up to 24 V (see “ Installation; Ignition Sense”).

Handset HSU–1 (optional)

An optional Handset offers more privacy during a call. The Holder is attached by screwing the Mounting Plate provided to the vehicle and sliding the Holder into place.

RS–232 Adapter Cable DLR–1 (optional)

The Adapter Cable is an optional connection between your PC and the Communicator.

External Mobile Antenna (not supplied)

The Hands–Free Car Kit is designed to operate with a high quality external antenna. However, due to many different types of antennas being available, an antenna is NOT included as part of this kit. Please, consult the dealer to find out which is the most suitable antena type for your installation.

Installation

There are some important aspects that require special attention in positioning Hands–Free Car Kit accessories.

The positioning of the Phone Holder is the most important factor when trying to achieve the most comfortable position for the user. The location of the Holder should be selected so that the visibility of the Communicator's display is good under all lighting conditions, but not so that the driver's attention is easily distracted. The Holder should be located so that the driver can easily reach the keypad. Under no circumstances should the Holder prevent the driver from controlling or operating the vehicle in any way or observing traffic.

The Junction Box can be installed in a hidden location, since there is no need to disconnect cables during normal operation. Ensure the location does not subject the unit and cables to moisture or mechanical pressure.

The Hands–Free Microphone should be installed according to the directions in the separate microphone installation guide. Ensure the microphone is as close to the driver's mouth as possible, and attached to a surface that is mechanically quiet. The microphone should be mounted at least 3 ft/1 m away from the Hands–Free Speaker to avoid acoustic feedback.

The Hands–Free Speaker is not very sensitive to vibrations, thus it can be located more freely. The main idea is to optimize two requirements: The driver should hear the signal from the loudspeaker without any special effort, but attenuation between the loudspeaker and the microphone should be as high as possible. That is, they must "look" in opposite directions in order to minimize the acoustic feedback.

Ensure cables are routed as far away as possible from the vehicle's electronic systems (refer to WARNINGS). In addition, ensure cables are not subjected to undue mechanical stress for example, under seats or against sharp edges. The charging holder should always be connected to the external mobile antenna via a non–radiating cable (for example, coaxial cable).

Car Radio Muting CRM

The Communicator offers a feature that can mute the car radio automatically during a conversation. This feature is convenient and provides for safer hands–free operation. The Car Radio Muting feature is based on a grounded line, so it means that in standby, the yellow wire (XCRM) is not grounded and car radio works normally, but during a call, line is grounded and car radio is muted. The maximum load that this line can handle is 250 mA. Note that an auxiliary relay or muting unit must be used when the car radio doesn't have a mute feature available.

When a relay is used this should be connected in series with the car radio main supply. A 200 mA fuse should be used to protect the XCRM output in event of a short circuit. Some radios have separate supplies for amplifiers and motors, and another for memory backup purposes. Very often these radios also have a secret code system, which activates itself if a break in the memory supply is detected. Be careful when installing the relay not to break the memory supply (usually marked ACC or +MEM), but to install the relay in the main supply feed.

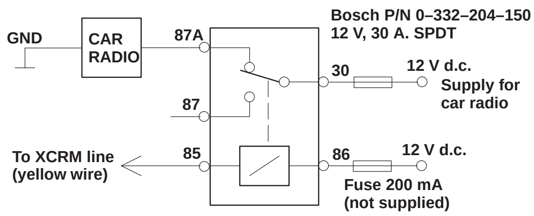

Figure 4. Radio Muting Circuit

Another possibility is to use a special muting unit, which mutes the radio by connecting load resistors to the speaker lines of the car radio. Four loudspeakers can be muted and the maximum permitted power is 20 watts per channel. The muting unit can also be used as a relay to cut the main supply feed of the car radio.

Ignition Sense IGNS

The Ignition Sense feature prevents your Communicator from draining the car battery by executing an auto power off in 20 seconds after the ignition key has been turned off. The blue wire of the power cable is used for the ignition sense feature. The use of ignition sense is recommended to prevent accidental draining of the car's battery. The wire is connected via a 200 mA fuse to a 12/24 volt potential that is controlled by the ignition key. Do not connect it directly to the high voltage sections of the ignition circuit.

All installations should take into account any special requirements of the customer. However, should the customer require an installation that is illegal or unsafe, these facts must be pointed out to the customer and a policy of non–compliance adopted.

Testing

Once installed, the equipment should be tested to ensure that it is operating satisfactorily and that the position of the units does not impair on the driver's ability to control and operate the vehicle in any way.

Use the Communicator to make a call when the vehicle is parked with the engine running. During the call, switch off the engine. Ensure that the phone is operational with the engine running and with the engine switched off. For operating information refer to the 'Accessories Guide' supplied with the Communicator.

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PARTS LISTS

CONTENTS – Parts lists

Note: *Common Modules for all versions are GP1 and GEM1*

Parts Lists

GSM System Module – GE8

EDMS pn 0200712 Issue 3.19

Item	Code	Description	Value/Type	
R200	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R201	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R202	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R206	1430726	Chip resistor	100	5 % 0.063 W 0402
R207	1430726	Chip resistor	100	5 % 0.063 W 0402
R208	1430726	Chip resistor	100	5 % 0.063 W 0402
R209	1430726	Chip resistor	100	5 % 0.063 W 0402
R210	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R211	1430700	Chip resistor	10	5 % 0.063 W 0402
R212	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R213	1430726	Chip resistor	100	5 % 0.063 W 0402
R216	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R220	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R222	1430726	Chip resistor	100	5 % 0.063 W 0402
R224	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R230	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R231	1430840	Chip resistor	220 k	1 % 0.063 W 0402
R232	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R233	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R250	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R251	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R252	1430115	Chip resistor	2.2 k	1 % 0.063 W 0402
R253	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R254	1430734	Chip resistor	220	5 % 0.063 W 0402
R255	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R256	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R257	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R258	1430732	Chip resistor	180	5 % 0.063 W 0402
R259	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R260	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R261	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R262	1430732	Chip resistor	180	5 % 0.063 W 0402
R263	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R264	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R265	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R266	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603

R267	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R268	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R270	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R271	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R300	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R301	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R302	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R303	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R304	1430730	Chip resistor	150	5 % 0.063 W 0402
R305	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R306	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R307	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R308	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R309	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R310	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R311	1430744	Chip resistor	470	5 % 0.063 W 0402
R312	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R313	1430115	Chip resistor	2.2 k	1 % 0.063 W 0402
R314	1430115	Chip resistor	2.2 k	1 % 0.063 W 0402
R320	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R330	1430722	Chip resistor	68	5 % 0.063 W 0402
R331	1430726	Chip resistor	100	5 % 0.063 W 0402
R332	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R333	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R334	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R335	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R336	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R337	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R338	1430726	Chip resistor	100	5 % 0.063 W 0402
R340	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R341	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R342	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R343	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R344	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R345	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R346	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R360	1430726	Chip resistor	100	5 % 0.063 W 0402
R361	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R362	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R363	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R364	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R365	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R366	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R367	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R370	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R372	1430798	Chip resistor	56 k	5 % 0.063 W 0402
R373	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R374	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R375	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R380	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R381	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R382	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R383	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R384	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R385	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R386	1430726	Chip resistor	100	5 % 0.063 W 0402
R387	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R388	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R389	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R390	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R391	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R400	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R401	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R402	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R403	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R404	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R405	1430700	Chip resistor	10	5 % 0.063 W 0402
R406	1430700	Chip resistor	10	5 % 0.063 W 0402
R407	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R408	1430726	Chip resistor	100	5 % 0.063 W 0402
R420	1430752	Chip resistor	820	5 % 0.063 W 0402
R421	1430726	Chip resistor	100	5 % 0.063 W 0402
R462	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R501	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R502	1430732	Chip resistor	180	5 % 0.063 W 0402
R503	1430732	Chip resistor	180	5 % 0.063 W 0402
R504	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R505	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R506	1430710	Chip resistor	22	5 % 0.063 W 0402
R507	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R508	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R509	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R511	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R512	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402

R513	1430740	Chip resistor	330	5 % 0.063 W 0402
R514	1430710	Chip resistor	22	5 % 0.063 W 0402
R541	1430710	Chip resistor	22	5 % 0.063 W 0402
R542	1430734	Chip resistor	220	5 % 0.063 W 0402
R543	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R544	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R545	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R546	1430724	Chip resistor	82	5 % 0.063 W 0402
R547	1430744	Chip resistor	470	5 % 0.063 W 0402
R551	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R552	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R553	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R554	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R555	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R556	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R557	1430730	Chip resistor	150	5 % 0.063 W 0402
R558	1430732	Chip resistor	180	5 % 0.063 W 0402
R559	1430740	Chip resistor	330	5 % 0.063 W 0402
R560	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R562	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R563	1430728	Chip resistor	120	5 % 0.063 W 0402
R564	1430738	Chip resistor	270	5 % 0.063 W 0402
R565	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R566	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R567	1430728	Chip resistor	120	5 % 0.063 W 0402
R568	1430734	Chip resistor	220	5 % 0.063 W 0402
R569	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R570	1430726	Chip resistor	100	5 % 0.063 W 0402
R571	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R572	1430276	Chip resistor	47 k	2 % 0.063 W 0603
R573	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R574	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R576	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R577	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R578	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R579	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R580	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R583	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R584	1430310	Chip resistor	75 k	2 % 0.063 W 0603
R601	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R602	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R603	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402

R701	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R702	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R703	1430710	Chip resistor	22	5 % 0.063 W 0402
R704	1430740	Chip resistor	330	5 % 0.063 W 0402
R705	1430724	Chip resistor	82	5 % 0.063 W 0402
R708	1430690	Chip jumper		0402
R711	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R712	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R713	1430744	Chip resistor	470	5 % 0.063 W 0402
R714	1430700	Chip resistor	10	5 % 0.063 W 0402
R715	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R716	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R717	1430734	Chip resistor	220	5 % 0.063 W 0402
R725	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R726	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R727	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R728	1430730	Chip resistor	150	5 % 0.063 W 0402
R736	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R737	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R738	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R739	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R740	1430115	Chip resistor	2.2 k	1 % 0.063 W 0402
R741	1430746	Chip resistor	560	5 % 0.063 W 0402
R742	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R743	1430700	Chip resistor	10	5 % 0.063 W 0402
R755	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R756	1412279	Chip resistor	2.2	5 % 0.1 W 0805
R765	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R766	1430748	Chip resistor	680	5 % 0.063 W 0402
R767	1430732	Chip resistor	180	5 % 0.063 W 0402
R768	1430752	Chip resistor	820	5 % 0.063 W 0402
R769	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R774	1430712	Chip resistor	27	5 % 0.063 W 0402
R775	1430712	Chip resistor	27	5 % 0.063 W 0402
R776	1430714	Chip resistor	33	5 % 0.063 W 0402
R780	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R781	1430740	Chip resistor	330	5 % 0.063 W 0402
R782	1430726	Chip resistor	100	5 % 0.063 W 0402
R783	1430690	Chip jumper		0402
R784	1430726	Chip resistor	100	5 % 0.063 W 0402
R785	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R800	1430778	Chip resistor	10 k	5 % 0.063 W 0402

R801	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R802	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R803	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R804	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R805	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R806	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R807	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R808	1430734	Chip resistor	220	5 % 0.063 W 0402
R809	1820024	NTC resistor	47 k	5 % 0.2 W 0805
R811	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R820	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R821	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R822	1430798	Chip resistor	56 k	5 % 0.063 W 0402
R823	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R824	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R825	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R826	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R827	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R828	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R829	1430718	Chip resistor	47	5 % 0.063 W 0402
R830	1430718	Chip resistor	47	5 % 0.063 W 0402
R840	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R841	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R842	1430844	Chip resistor	3.9 k	1 % 0.063 W 0402
R843	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R844	1430734	Chip resistor	220	5 % 0.063 W 0402
R845	1430700	Chip resistor	10	5 % 0.063 W 0402
R846	1430726	Chip resistor	100	5 % 0.063 W 0402
R847	1430718	Chip resistor	47	5 % 0.063 W 0402
R860	1430716	Chip resistor	39	5 % 0.063 W 0402
C200	2310336	Ceramic cap.	18 p	5 % 50 V 0805
C201	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C202	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C203	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C204	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C205	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C206	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C207	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C210	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C211	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C212	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C213	2320131	Ceramic cap.	33 n	10 % 16 V 0603

C214	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C215	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C216	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C217	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C218	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C219	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C220	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C221	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C225	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C230	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C231	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C232	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C233	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C234	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C235	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C236	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C237	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C238	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C239	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C240	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C241	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C242	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C243	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C244	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C245	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C246	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C247	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C248	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C249	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C250	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C251	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C252	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C253	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C300	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C301	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C302	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C303	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C304	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C305	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C306	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C307	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C308	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C309	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C320	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C321	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C322	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C323	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C324	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C325	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C326	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C330	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C331	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C332	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C333	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C340	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C341	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C342	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C343	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C345	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C346	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C347	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C348	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C349	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C350	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C360	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C361	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C362	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C363	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C380	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C381	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C382	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C383	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C384	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C385	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C386	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C387	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C388	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C389	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C390	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C391	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C392	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C393	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C394	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C395	2320620	Ceramic cap.	10 n	5 % 16 V 0402

C396	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C400	2312292	Ceramic cap.	470 n	20 % Y5 V 1210
C401	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C402	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C403	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C404	2610128	Tantalum cap.	10 u	20 % 3.5x2.8x1.9
C405	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C406	2604209	Tantalum cap.	1.0 u	20 % 16 V 3.2x1.6x1.6
C407	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C408	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C409	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C410	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C411	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C412	2604199	Tantalum cap.	2.2 u	20 % 3.2x1.6x1.6
C413	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C414	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C415	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C416	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C417	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C418	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C420	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C421	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C422	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C423	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C424	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C425	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C426	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C430	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C431	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C432	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C433	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C434	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C435	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C436	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C437	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C501	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C502	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C503	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C504	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C505	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C506	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C511	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402

C512	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C513	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C514	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C515	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C516	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C517	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C521	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C536	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C541	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C542	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C543	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C544	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C545	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C546	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C551	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C552	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C553	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C554	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C555	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C556	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C557	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C558	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C559	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C560	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C561	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C562	2320075	Ceramic cap.	470 p	5 % 50 V 0603
C563	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C564	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C565	2310470	Ceramic cap.	270 p	5 % 50 V 0805
C566	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C567	2310470	Ceramic cap.	270 p	5 % 50 V 0805
C569	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C570	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C571	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C572	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C573	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C574	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C575	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C580	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C601	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C602	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C603	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206

C604	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C605	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C606	2310752	Ceramic cap.	10 n	20 % 50 V 0805
C607	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C608	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C609	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C701	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C702	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C703	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C704	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C705	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C710	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C711	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C712	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C713	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C716	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C720	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C721	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C722	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C723	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C725	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C726	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C728	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C729	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C730	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C731	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C732	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C735	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C736	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C737	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C738	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C739	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C740	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C741	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C742	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C743	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C744	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C755	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C756	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C757	2320580	Ceramic cap.	680 p	5 % 50 V 0402
C758	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C759	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402

C760	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C761	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C762	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C763	2610011	Tantalum cap.	330 u	10 % 10 V 6.9x6x3.5
C764	2320361	Ceramic cap.	18 p	2 % 25 V 0603
C768	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C770	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C780	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C781	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C782	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C783	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C784	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C790	2610011	Tantalum cap.	330 u	10 % 10 V 6.9x6x3.5
C791	2610011	Tantalum cap.	330 u	10 % 10 V 6.9x6x3.5
C792	2610011	Tantalum cap.	330 u	10 % 10 V 6.9x6x3.5
C793	2610011	Tantalum cap.	330 u	10 % 10 V 6.9x6x3.5
C800	2604079	Tantalum cap.	0.22 u	20 % 35 V 3.2x1.6x1.6
C801	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C803	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C804	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C805	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C806	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C807	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C808	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C809	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C810	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C821	2310167	Ceramic cap.	1.0 n	5 % 50 V 1206
C822	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C823	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C824	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C828	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C829	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C830	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C831	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C832	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C840	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C841	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C843	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C844	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C845	2320604	Ceramic cap.	18 p	5 % 50 V 0402

C846	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C847	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C848	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C849	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C850	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C851	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C862	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C863	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
L200	3641262	Ferrite bead 30r/100mhz 2a 1206		
L201	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
L202	3641262	Ferrite bead 30r/100mhz 2a 1206		
L203	3641548	Chip coil 100 n 10 % Q=40/150 MHz		
L230	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
L231	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
L232	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
L300	3641302	Chip coil	470 n	5 % Q=30/25 MHz 1008
L511	3641550	Chip coil	120 n	10 % Q=35/150 MHz
L532	3641550	Chip coil	120 n	10 % Q=35/150 MHz
L541	3641550	Chip coil	120 n	10 % Q=35/150 MHz
L542	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L543	3641560	Chip coil	220 n	10 % Q=30/100 MHz
L544	3641560	Chip coil	220 n	10 % Q=30/100 MHz
L545	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L546	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L551	3641538	Chip coil	39 n	20 % Q=40/250 MHz
L700	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
L705	3640013	Chip coil	8 n	5 % Q=50/250 MHz
L710	3641622	Chip coil	220 n	5 % Q=30/100 MHz
L711	3641542	Chip coil	56 n	10 % Q=40/200 MHz
L800	3641206	Chip coil		10 % Q=25/7.96 MHz
L801	3641206	Chip coil		10 % Q=25/7.96 MHz
L840	3641574	Chip coil	68 n	5 % Q=40/200 MHz
L841	3641538	Chip coil	39 n	20 % Q=40/250 MHz
B800	4510071	Crystal	26.000 M	
G001	4352933	Vco 1006–1031mhz4.5v 15ma		
G300	4510044	Crystal	60.2 M	
Z500	4512046	Dupl 890–915/935–960mhz		
Z505	4511016	Saw filter	947.5+–12.5 M	
Z541	4511026	Saw filter	71+–0.08 M	
Z551	4510009	Cer.filt 13+–0.09mhz 330r		
Z713	4550101	Cer.filt 902.5+–12.5mhz		
T300	3640402	Transformer 4:1 balun 800mhz smd		

V200	4111824	Diode	BAS16	75V 250 mA 6 ns SOT23
V201	4111824	Diode	BAS16	75V 250 mA 6 ns SOT23
V202	4100285	Diode x 2	BAV99	70V200mASER.SOT23
V230	4210020	Transistor	BCP69–25pnp 20 V 1 A SOT223	
V231	4200877	Transistor	BCX51–16pnp 45 V 1.5 A SOT89	
V232	4210020	Transistor	BCP69–25pnp 20 V 1 A SOT223	
V250	4210020	Transistor	BCP69–25pnp 20 V 1 A SOT223	
V251	4110074	Schottky diode	STPS340U40 V 3 A SOD6	
V253	4200226	Darl. transistor	BCV27npn 30 V 300 mA SOT23	
V254	4200226	Darl. transistor	BCV27 npn 30 V 300 mA SOT23	
V255	4200909	Transistor	BC858B/BCW30 pnp 30V 100mA SOT23	
V256	4110126	Zener diode	BZX84	5 % 4.3V 0.3 W SOT23
V257	4202671	MosFet	BST82	n–ch 80V 175mA SOT23
V300	4210079	Transistor	BFS17	npn 15V 50mA SOT23
V301	4210079	Transistor	BFS17	npn 15V 50mA SOT23
V302	4210050	Transistor	DTA114EE pnp RB V EM3	
V303	4210100	Transistor	BC848W	npn 30 V SOT323
V320	4110014	Sch. diode x 2	BAS70–07 70V 15mA SOT143	
V330	4210100	Transistor	BC848W	npn 30 V SOT323
V331	4200909	Transistor	BC858B/BCW30 pnp 30V 100mA SOT23	
V370	4210102	Transistor	BC858W pnp 30V100mA 200MWSOT323	
V380	4200829	Transistor	BC859C	pnp 30 V 0.1 A SOT23
V381	4200811	Transistor	BC849C	npn 30 V 0.1 A SOT23
V400	4200917	Transistor	BC848B/BCW32 npn 30V 100 mA SOT23	
V420	4117998	Precision voltage reference 4.096		4.096
V460	4110014	Sch. diode x 2	BAS70–07 70V 15mA SOT143	
V501	4210046	Transistor	BFP182	npn 20V 35mA SOT143
V502	4210102	Transistor	BC858W	pnp 30V 100mA 200MWSOT323
V503	4210100	Transistor	BC848W	npn 30 V SOT323
V511	4115802	Sch. diode x 2	4V	30 mA SOT23
V512	4210066	Transistor	BFR93AW npn12 V35mA SOT323	
V541	4210066	Transistor	BFR93AWnpn 12V 35mA SOT323	
V701	4210066	Transistor	BFR93AWnpn 12V 35mA SOT323	
V702	4100567	Sch. diode x 2	BAS70–04 70V 15mA SERSOT23	
V710	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23
V725	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23

V726	4210102	Transistor	BC858W pnp 30V 100mA 200MWSOT323
V735	4210100	Transistor	BC848W npn 30V SOT323
V736	4217070	Transistor x 2	IMD
V737	4210102	Transistor	BC858W pnp 30V 100mA 200MWSOT323
V738	4210090	Transistor	BFG540/X npn 15V 129mA SOT143
V755	4210102	Transistor	BC858W pnp 30V 100mA 200MWSOT323
V756	4210133	Transistor	BFG10W/X npn 10V 0.25A SOT343
V765	4210100	Transistor	BC848W npn 30 V SOT323
V766	4210100	Transistor	BC848W npn 30 V SOT323
V767	4100285	Diode x 2	BAV99 70V 200mA SER.SOT23
V768	4210135	Transistor	BLT82 npn 10 V SO8S
V780	4110014	Sch. diode x 2	BAS70–07 70V 15mA SOT143
V800	4110081	Cap. diode	BB640 28/1 V SOD323
V801	4210066	Transistor	BFR93AW npn12V 35mA SOT323
V802	4210066	Transistor	BFR93AW npn12V 35mA SOT323
V840	4210066	Transistor	BFR93AW npn12V 35mA SOT323
V841	4210066	Transistor	BFR93AW npn12V 35mA SOT323
V842	4110018	Cap. diode	BB135 30 V SOD323
D300	4340126	IC, 1xnand 2input cmos ss TC7S00FSSO5	
D301	4340126	IC, 1xnand 2input cmos ssTC7S00FSSO5	
N230	4375588	IC, PSL+ power supply SO24W	
N400	4340303	IC, af amp 0.5w 2.7–5.5v soLM4861 SO8S	
N551	4370091	Crfrt_st tx.mod+rxif+pwc sqfp44 SQFP44	
N601	4370095	Crfcontf 8xreg4.5v vref2v5 vsop28 VSOP28	
N820	4340005	IC, 2xsynth 1.2ghz 3v sso UMA1018MSSO20	
X201	5469203	SM, conn 2x22 f p0.8 pcb/pcb 9.0 9.0MM	
X202	5409041	SM, conn battery 4pol p2.54	
X212	5469037	SM, flex conn 12pol p0.5 u.conta U.CONTACT	
X400	5469031	SM, conn chp2502–0101 1x2 m p1.2	
X501	5429003	SM, coax conn recep 50r 3ghz 5x4	
X503	5420460	Coax–conn female 50ohm switch ims	
MCM1	0200725	Submodule	
MCM2	0200726	Submodule	
	9854110	PCB GE8 121X55X1.0 M6 2/PA	

PCN System Module – GE9_05

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Item	Code	Description / Value / Type
R200	1430796	CHIPRES 0W06 47K J 0402
R201	1430804	CHIPRES 0W06 100K J 0402
R202	1430788	CHIPRES 0W06 22K J 0402
R206	1430726	CHIPRES 0W06 100R J 0402
R207	1430726	CHIPRES 0W06 100R J 0402
R208	1430726	CHIPRES 0W06 100R J 0402
R209	1430726	CHIPRES 0W06 100R J 0402
R210	1430796	CHIPRES 0W06 47K J 0402
R211	1430700	CHIPRES 0W06 10R J 0402
R212	1430804	CHIPRES 0W06 100K J 0402
R213	1430726	CHIPRES 0W06 100R J 0402
R216	1430778	CHIPRES 0W06 10K J 0402
R220	1430770	CHIPRES 0W06 4K7 J 0402
R222	1430726	CHIPRES 0W06 100R J 0402
R224	1430079	CHIPRES 0W06 47K J 0603
R230	1430842	CHIPRES 0W06 680K F 0402
R231	1430840	CHIPRES 0W06 220K F 0402
R232	1430804	CHIPRES 0W06 100K J 0402
R233	1430804	CHIPRES 0W06 100K J 0402
R250	1430792	CHIPRES 0W06 33K J 0402
R251	1430764	CHIPRES 0W06 3K3 J 0402
R252	1430846	CHIPRES 0W06 2K7 F 0402
R253	1430764	CHIPRES 0W06 3K3 J 0402
R254	1430734	CHIPRES 0W06 220R J 0402
R255	1430788	CHIPRES 0W06 22K J 0402
R256	1430844	CHIPRES 0W06 3K9 F 0402
R257	1430778	CHIPRES 0W06 10K J 0402
R258	1430732	CHIPRES 0W06 180R J 0402
R259	1430804	CHIPRES 0W06 100K J 0402
R260	1430762	CHIPRES 0W06 2K2 J 0402
R261	1430762	CHIPRES 0W06 2K2 J 0402
R262	1430732	CHIPRES 0W06 180R J 0402
R263	1430778	CHIPRES 0W06 10K J 0402
R264	1430778	CHIPRES 0W06 10K J 0402
R265	1430045	CHIPRES 0W06 2K7 J 0603
R266	1430045	CHIPRES 0W06 2K7 J 0603
R267	1430087	CHIPRES 0W06 100K J 0603
R268	1430087	CHIPRES 0W06 100K J 0603

R270	1430776	CHIPRES 0W06 8K2 J	0402
R271	1430812	CHIPRES 0W06 220K J	0402
R300	1430762	CHIPRES 0W06 2K2 J	0402
R301	1430804	CHIPRES 0W06 100K J	0402
R302	1430804	CHIPRES 0W06 100K J	0402
R303	1430754	CHIPRES 0W06 1K0 J	0402
R304	1430730	CHIPRES 0W06 150R J	0402
R305	1430804	CHIPRES 0W06 100K J	0402
R306	1430788	CHIPRES 0W06 22K J	0402
R307	1430794	CHIPRES 0W06 39K J	0402
R308	1430804	CHIPRES 0W06 100K J	0402
R309	1430796	CHIPRES 0W06 47K J	0402
R310	1430764	CHIPRES 0W06 3K3 J	0402
R311	1430744	CHIPRES 0W06 470R J	0402
R312	1430796	CHIPRES 0W06 47K J	0402
R313	1430115	CHIPRES 0W06 2K2 F 200PPM	0402
R314	1430115	CHIPRES 0W06 2K2 F 200PPM	0402
R320	1430804	CHIPRES 0W06 100K J	0402
R330	1430722	CHIPRES 0W06 68R J	0402
R331	1430726	CHIPRES 0W06 100R J	0402
R332	1430804	CHIPRES 0W06 100K J	0402
R333	1430770	CHIPRES 0W06 4K7 J	0402
R334	1430760	CHIPRES 0W06 1K8 J	0402
R335	1430804	CHIPRES 0W06 100K J	0402
R336	1430792	CHIPRES 0W06 33K J	0402
R337	1430778	CHIPRES 0W06 10K J	0402
R338	1430726	CHIPRES 0W06 100R J	0402
R340	1430762	CHIPRES 0W06 2K2 J	0402
R341	1430762	CHIPRES 0W06 2K2 J	0402
R342	1430762	CHIPRES 0W06 2K2 J	0402
R343	1430762	CHIPRES 0W06 2K2 J	0402
R344	1430762	CHIPRES 0W06 2K2 J	0402
R345	1430762	CHIPRES 0W06 2K2 J	0402
R346	1430762	CHIPRES 0W06 2K2 J	0402
R360	1430726	CHIPRES 0W06 100R J	0402
R361	1430754	CHIPRES 0W06 1K0 J	0402
R362	1430754	CHIPRES 0W06 1K0 J	0402
R363	1430754	CHIPRES 0W06 1K0 J	0402
R364	1430754	CHIPRES 0W06 1K0 J	0402
R365	1430754	CHIPRES 0W06 1K0 J	0402
R366	1430754	CHIPRES 0W06 1K0 J	0402
R367	1430754	CHIPRES 0W06 1K0 J	0402

R370	1430796	CHIPRES 0W06 47K J	0402
R372	1430798	CHIPRES 0W06 56K J	0402
R373	1430804	CHIPRES 0W06 100K J	0402
R374	1430826	CHIPRES 0W06 680K J	0402
R375	1430804	CHIPRES 0W06 100K J	0402
R380	1430804	CHIPRES 0W06 100K J	0402
R381	1430804	CHIPRES 0W06 100K J	0402
R382	1430778	CHIPRES 0W06 10K J	0402
R383	1430792	CHIPRES 0W06 33K J	0402
R384	1430754	CHIPRES 0W06 1K0 J	0402
R385	1430754	CHIPRES 0W06 1K0 J	0402
R386	1430726	CHIPRES 0W06 100R J	0402
R387	1430784	CHIPRES 0W06 15K J	0402
R388	1430778	CHIPRES 0W06 10K J	0402
R389	1430754	CHIPRES 0W06 1K0 J	0402
R390	1430754	CHIPRES 0W06 1K0 J	0402
R391	1430760	CHIPRES 0W06 1K8 J	0402
R400	1430796	CHIPRES 0W06 47K J	0402
R401	1430778	CHIPRES 0W06 10K J	0402
R402	1430778	CHIPRES 0W06 10K J	0402
R403	1430778	CHIPRES 0W06 10K J	0402
R404	1430778	CHIPRES 0W06 10K J	0402
R405	1430700	CHIPRES 0W06 10R J	0402
R406	1430700	CHIPRES 0W06 10R J	0402
R407	1430804	CHIPRES 0W06 100K J	0402
R408	1430726	CHIPRES 0W06 100R J	0402
R420	1430752	CHIPRES 0W06 820R J	0402
R421	1430726	CHIPRES 0W06 100R J	0402
R462	1430754	CHIPRES 0W06 1K0 J	0402
R500	1430690	CHIPRES JUMPER 0R0	0402
R501	1430770	CHIPRES 0W06 4K7 J	0402
R502	1430732	CHIPRES 0W06 180R J	0402
R503	1430728	CHIPRES 0W06 120R J	0402
R504	1430778	CHIPRES 0W06 10K J	0402
R505	1430772	CHIPRES 0W06 5K6 J	0402
R506	1430710	CHIPRES 0W06 22R J	0402
R507	1430804	CHIPRES 0W06 100K J	0402
R508	1430804	CHIPRES 0W06 100K J	0402
R509	1430774	CHIPRES 0W06 6K8 J	0402
R510	1430762	CHIPRES 0W06 2K2 J	0402
R511	1430770	CHIPRES 0W06 4K7 J	0402
R512	1430832	CHIPRES 0W06 2K7 J	0402

R513	1430744	CHIPRES 0W06 470R J	0402
R514	1430710	CHIPRES 0W06 22R J	0402
R518	1430778	CHIPRES 0W06 10K J	0402
R521	1430754	CHIPRES 0W06 1K0 J	0402
R522	1430762	CHIPRES 0W06 2K2 J	0402
R523	1430756	CHIPRES 0W06 1K2 J	0402
R524	1430734	CHIPRES 0W06 220R J	0402
R525	1430734	CHIPRES 0W06 220R J	0402
R531	1430710	CHIPRES 0W06 22R J	0402
R532	1430740	CHIPRES 0W06 330R J	0402
R533	1430770	CHIPRES 0W06 4K7 J	0402
R534	1430832	CHIPRES 0W06 2K7 J	0402
R535	1430710	CHIPRES 0W06 22R J	0402
R541	1430710	CHIPRES 0W06 22R J	0402
R543	1430740	CHIPRES 0W06 330R J	0402
R544	1430762	CHIPRES 0W06 2K2 J	0402
R545	1430758	CHIPRES 0W06 1K5 J	0402
R546	1430724	CHIPRES 0W06 82R J	0402
R547	1430744	CHIPRES 0W06 470R J	0402
R548	1430734	CHIPRES 0W06 220R J	0402
R549	1430778	CHIPRES 0W06 10K J	0402
R550	1430778	CHIPRES 0W06 10K J	0402
R551	1430770	CHIPRES 0W06 4K7 J	0402
R552	1430788	CHIPRES 0W06 22K J	0402
R553	1430770	CHIPRES 0W06 4K7 J	0402
R554	1430770	CHIPRES 0W06 4K7 J	0402
R555	1430788	CHIPRES 0W06 22K J	0402
R556	1430770	CHIPRES 0W06 4K7 J	0402
R557	1430730	CHIPRES 0W06 150R J	0402
R558	1430732	CHIPRES 0W06 180R J	0402
R559	1430740	CHIPRES 0W06 330R J	0402
R560	1430764	CHIPRES 0W06 3K3 J	0402
R561	1430792	CHIPRES 0W06 33K J	0402
R562	1430754	CHIPRES 0W06 1K0 J	0402
R563	1430728	CHIPRES 0W06 120R J	0402
R564	1430738	CHIPRES 0W06 270R J	0402
R565	1430754	CHIPRES 0W06 1K0 J	0402
R566	1430754	CHIPRES 0W06 1K0 J	0402
R567	1430728	CHIPRES 0W06 120R J	0402
R568	1430734	CHIPRES 0W06 220R J	0402
R569	1430754	CHIPRES 0W06 1K0 J	0402
R570	1430726	CHIPRES 0W06 100R J	0402

R571	1430762	CHIPRES 0W06 2K2 J	0402
R572	1430276	CHIPRES 0W06 47K G	0603
R573	1430778	CHIPRES 0W06 10K J	0402
R574	1430778	CHIPRES 0W06 10K J	0402
R576	1430770	CHIPRES 0W06 4K7 J	0402
R577	1430792	CHIPRES 0W06 33K J	0402
R578	1430794	CHIPRES 0W06 39K J	0402
R579	1430778	CHIPRES 0W06 10K J	0402
R580	1430790	CHIPRES 0W06 27K J	0402
R584	1430310	CHIPRES 0W06 75K G	0603
R601	1430762	CHIPRES 0W06 2K2 J	0402
R602	1430762	CHIPRES 0W06 2K2 J	0402
R603	1430762	CHIPRES 0W06 2K2 J	0402
R701	1430832	CHIPRES 0W06 2K7 J	0402
R702	1430770	CHIPRES 0W06 4K7 J	0402
R703	1430710	CHIPRES 0W06 22R J	0402
R704	1430740	CHIPRES 0W06 330R J	0402
R705	1430730	CHIPRES 0W06 150R J	0402
R706	1430693	CHIPRES 0W06 5R6 J	0402
R707	1430730	CHIPRES 0W06 150R J	0402
R710	1430690	CHIPRES JUMPER 0R0	0402
R711	1430758	CHIPRES 0W06 1K5 J	0402
R712	1430832	CHIPRES 0W06 2K7 J	0402
R713	1430744	CHIPRES 0W06 470R J	0402
R714	1430700	CHIPRES 0W06 10R J	0402
R715	1430730	CHIPRES 0W06 150R J	0402
R716	1430700	CHIPRES 0W06 10R J	0402
R725	1430784	CHIPRES 0W06 15K J	0402
R726	1430788	CHIPRES 0W06 22K J	0402
R727	1430762	CHIPRES 0W06 2K2 J	0402
R728	1430728	CHIPRES 0W06 120R J	0402
R729	1430730	CHIPRES 0W06 150R J	0402
R730	1430700	CHIPRES 0W06 10R J	0402
R731	1430728	CHIPRES 0W06 120R J	0402
R732	1430700	CHIPRES 0W06 10R J	0402
R735	1430762	CHIPRES 0W06 2K2 J	0402
R737	1430756	CHIPRES 0W06 1K2 J	0402
R738	1430778	CHIPRES 0W06 10K J	0402
R739	1430778	CHIPRES 0W06 10K J	0402
R740	1430774	CHIPRES 0W06 6K8 J	0402
R741	1430764	CHIPRES 0W06 3K3 J	0402
R742	1430774	CHIPRES 0W06 6K8 J	0402

R743	1430762	CHIPRES 0W06 2K2 J	0402
R744	1430762	CHIPRES 0W06 2K2 J	0402
R745	1430762	CHIPRES 0W06 2K2 J	0402
R746	1430756	CHIPRES 0W06 1K2 J	0402
R747	1430712	CHIPRES 0W06 27R J	0402
R748	1430754	CHIPRES 0W06 1K0 J	0402
R749	1430732	CHIPRES 0W06 180R J	0402
R750	1430754	CHIPRES 0W06 1K0 J	0402
R751	1430778	CHIPRES 0W06 10K J	0402
R755	1430762	CHIPRES 0W06 2K2 J	0402
R756	1430754	CHIPRES 0W06 1K0 J	0402
R757	1430734	CHIPRES 0W06 220R J	0402
R758	1412279	CHIPRES 0W1 2R2 J	0805
R765	1430762	CHIPRES 0W06 2K2 J	0402
R766	1430754	CHIPRES 0W06 1K0 J	0402
R767	1430726	CHIPRES 0W06 100R J	0402
R768	1411123	MELFRES 0W25 0R22 J	0204
R774	1430712	CHIPRES 0W06 27R J	0402
R775	1430712	CHIPRES 0W06 27R J	0402
R776	1430714	CHIPRES 0W06 33R J	0402
R780	1430770	CHIPRES 0W06 4K7 J	0402
R781	1430740	CHIPRES 0W06 330R J	0402
R782	1430726	CHIPRES 0W06 100R J	0402
R783	1430722	CHIPRES 0W06 68R J	0402
R784	1430726	CHIPRES 0W06 100R J	0402
R785	1430762	CHIPRES 0W06 2K2 J	0402
R790	1430700	CHIPRES 0W06 10R J	0402
R791	1430718	CHIPRES 0W06 47R J	0402
R792	1430770	CHIPRES 0W06 4K7 J	0402
R800	1430778	CHIPRES 0W06 10K J	0402
R801	1430796	CHIPRES 0W06 47K J	0402
R802	1430796	CHIPRES 0W06 47K J	0402
R803	1430762	CHIPRES 0W06 2K2 J	0402
R804	1430788	CHIPRES 0W06 22K J	0402
R805	1430786	CHIPRES 0W06 18K J	0402
R806	1430774	CHIPRES 0W06 6K8 J	0402
R807	1430758	CHIPRES 0W06 1K5 J	0402
R808	1430734	CHIPRES 0W06 220R J	0402
R809	1820024	NTC RES 0W2 47K J B=4050+–3%	0805
R820	1430778	CHIPRES 0W06 10K J	0402
R821	1430786	CHIPRES 0W06 18K J	0402
R822	1430778	CHIPRES 0W06 10K J	0402

R823	1430770	CHIPRES 0W06 4K7 J	0402
R824	1430770	CHIPRES 0W06 4K7 J	0402
R825	1430770	CHIPRES 0W06 4K7 J	0402
R827	1430766	CHIPRES 0W06 3K9 J	0402
R828	1430786	CHIPRES 0W06 18K J	0402
R829	1430718	CHIPRES 0W06 47R J	0402
R830	1430718	CHIPRES 0W06 47R J	0402
R840	1430786	CHIPRES 0W06 18K J	0402
R841	1430770	CHIPRES 0W06 4K7 J	0402
R842	1430770	CHIPRES 0W06 4K7 J	0402
R843	1430832	CHIPRES 0W06 2K7 J	0402
R844	1430734	CHIPRES 0W06 220R J	0402
R845	1430700	CHIPRES 0W06 10R J	0402
R846	1430710	CHIPRES 0W06 22R J	0402
R847	1430718	CHIPRES 0W06 47R J	0402
R860	1430716	CHIPRES 0W06 39R J	0402
C200	2310336	CHIPCAP NP0 18P J 50V	0805
C201	2320544	CHIPCAP NP0 22P J 50V	0402
C202	2320744	CHIPCAP X7R 1N0 K 50V	0402
C203	2320744	CHIPCAP X7R 1N0 K 50V	0402
C204	2320778	CHIPCAP X7R 10N K 16V	0402
C205	2320778	CHIPCAP X7R 10N K 16V	0402
C206	2320560	CHIPCAP NP0 100P J 50V	0402
C207	2320560	CHIPCAP NP0 100P J 50V	0402
C210	2320131	CHIPCAP X7R 33N K 16V	0603
C211	2320131	CHIPCAP X7R 33N K 16V	0603
C212	2320131	CHIPCAP X7R 33N K 16V	0603
C213	2320131	CHIPCAP X7R 33N K 16V	0603
C214	2320131	CHIPCAP X7R 33N K 16V	0603
C215	2320131	CHIPCAP X7R 33N K 16V	0603
C216	2320131	CHIPCAP X7R 33N K 16V	0603
C217	2320131	CHIPCAP X7R 33N K 16V	0603
C218	2320131	CHIPCAP X7R 33N K 16V	0603
C219	2320131	CHIPCAP X7R 33N K 16V	0603
C220	2320744	CHIPCAP X7R 1N0 K 50V	0402
C221	2320544	CHIPCAP NP0 22P J 50V	0402
C225	2320107	CHIPCAP X7R 10N J 50V	0603
C230	2320560	CHIPCAP NP0 100P J 50V	0402
C231	2320620	CHIPCAP X7R 10N J 16V	0402
C232	2604209	CHIPTCAP 1U0 M 16V	3.2X1.6X1.6
C233	2604209	CHIPTCAP 1U0 M 16V	3.2X1.6X1.6
C234	2320744	CHIPCAP X7R 1N0 K 50V	0402

C235	2310791	CHIPCAP X7R 33N M 50V	0805
C236	2320620	CHIPCAP X7R 10N J 16V	0402
C237	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C238	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C239	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C240	2320778	CHIPCAP X7R 10N K 16V	0402
C241	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C242	2320560	CHIPCAP NP0 100P J 50V	0402
C243	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C244	2604329	CHIPTCAP 4U7 M 10V	3.5X2.8X1.9
C245	2320560	CHIPCAP NP0 100P J 50V	0402
C246	2320620	CHIPCAP X7R 10N J 16V	0402
C247	2320560	CHIPCAP NP0 100P J 50V	0402
C248	2320560	CHIPCAP NP0 100P J 50V	0402
C249	2320107	CHIPCAP X7R 10N J 50V	0603
C250	2320107	CHIPCAP X7R 10N J 50V	0603
C251	2604209	CHIPTCAP 1U0 M 16V	3.2X1.6X1.6
C252	2320598	CHIPCAP X7R 3N9 J 50V	0402
C253	2320620	CHIPCAP X7R 10N J 16V	0402
C296	2320560	CHIPCAP NP0 100P J 50V	0402
C300	2320598	CHIPCAP X7R 3N9 J 50V	0402
C301	2320598	CHIPCAP X7R 3N9 J 50V	0402
C302	2320598	CHIPCAP X7R 3N9 J 50V	0402
C303	2320598	CHIPCAP X7R 3N9 J 50V	0402
C304	2320544	CHIPCAP NP0 22P J 50V	0402
C305	2320544	CHIPCAP NP0 22P J 50V	0402
C306	2320560	CHIPCAP NP0 100P J 50V	0402
C307	2320598	CHIPCAP X7R 3N9 J 50V	0402
C308	2320560	CHIPCAP NP0 100P J 50V	0402
C309	2320560	CHIPCAP NP0 100P J 50V	0402
C320	2320560	CHIPCAP NP0 100P J 50V	0402
C321	2320544	CHIPCAP NP0 22P J 50V	0402
C322	2320544	CHIPCAP NP0 22P J 50V	0402
C323	2320560	CHIPCAP NP0 100P J 50V	0402
C324	2320560	CHIPCAP NP0 100P J 50V	0402
C325	2320560	CHIPCAP NP0 100P J 50V	0402
C326	2320560	CHIPCAP NP0 100P J 50V	0402
C330	2320560	CHIPCAP NP0 100P J 50V	0402
C331	2320536	CHIPCAP NP0 10P J 50V	0402
C332	2320620	CHIPCAP X7R 10N J 16V	0402
C333	2320536	CHIPCAP NP0 10P J 50V	0402
C340	2320560	CHIPCAP NP0 100P J 50V	0402

C341	2320560	CHIPCAP NP0 100P J 50V	0402
C342	2320560	CHIPCAP NP0 100P J 50V	0402
C343	2320560	CHIPCAP NP0 100P J 50V	0402
C345	2320560	CHIPCAP NP0 100P J 50V	0402
C346	2320552	CHIPCAP NP0 47P J 50V	0402
C347	2320560	CHIPCAP NP0 100P J 50V	0402
C348	2320560	CHIPCAP NP0 100P J 50V	0402
C349	2320560	CHIPCAP NP0 100P J 50V	0402
C350	2320560	CHIPCAP NP0 100P J 50V	0402
C360	2320544	CHIPCAP NP0 22P J 50V	0402
C361	2320560	CHIPCAP NP0 100P J 50V	0402
C362	2320560	CHIPCAP NP0 100P J 50V	0402
C363	2320560	CHIPCAP NP0 100P J 50V	0402
C380	2320560	CHIPCAP NP0 100P J 50V	0402
C381	2604209	CHIPTCAP 1U0 M 16V	3.2X1.6X1.6
C382	2320604	CHIPCAP NP0 18P J 50V	0402
C383	2320604	CHIPCAP NP0 18P J 50V	0402
C384	2320131	CHIPCAP X7R 33N K 16V	0603
C385	2320131	CHIPCAP X7R 33N K 16V	0603
C386	2320131	CHIPCAP X7R 33N K 16V	0603
C387	2320131	CHIPCAP X7R 33N K 16V	0603
C388	2320131	CHIPCAP X7R 33N K 16V	0603
C389	2320560	CHIPCAP NP0 100P J 50V	0402
C390	2320560	CHIPCAP NP0 100P J 50V	0402
C391	2320560	CHIPCAP NP0 100P J 50V	0402
C392	2320560	CHIPCAP NP0 100P J 50V	0402
C393	2320560	CHIPCAP NP0 100P J 50V	0402
C394	2320131	CHIPCAP X7R 33N K 16V	0603
C395	2320620	CHIPCAP X7R 10N J 16V	0402
C396	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C400	2312292	CHIPCAP Y5V 470N M 50V	1210
C401	2320598	CHIPCAP X7R 3N9 J 50V	0402
C402	2320584	CHIPCAP X7R 1N0 J 50V	0402
C403	2320544	CHIPCAP NP0 22P J 50V	0402
C404	2610128	CHIPTCAP 10U M 6V3	3.5X2.8X1.9
C405	2310784	CHIPCAP X7R 100N K 25V	0805
C406	2604209	CHIPTCAP 1U0 M 16V	3.2X1.6X1.6
C407	2310784	CHIPCAP X7R 100N K 25V	0805
C408	2320544	CHIPCAP NP0 22P J 50V	0402
C409	2320544	CHIPCAP NP0 22P J 50V	0402
C410	2320544	CHIPCAP NP0 22P J 50V	0402
C411	2320544	CHIPCAP NP0 22P J 50V	0402

C412	2604199	CHIPTCAP 2U2 M 6V3	3.2X1.6X1.6
C413	2320620	CHIPCAP X7R 10N J 16V	0402
C414	2320620	CHIPCAP X7R 10N J 16V	0402
C415	2320744	CHIPCAP X7R 1N0 K 50V	0402
C416	2320744	CHIPCAP X7R 1N0 K 50V	0402
C417	2320544	CHIPCAP NP0 22P J 50V	0402
C418	2320544	CHIPCAP NP0 22P J 50V	0402
C420	2320544	CHIPCAP NP0 22P J 50V	0402
C421	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C422	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C423	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C424	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C425	2320131	CHIPCAP X7R 33N K 16V	0603
C426	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C430	2320131	CHIPCAP X7R 33N K 16V	0603
C431	2320131	CHIPCAP X7R 33N K 16V	0603
C432	2320131	CHIPCAP X7R 33N K 16V	0603
C433	2310791	CHIPCAP X7R 33N M 50V	0805
C434	2310791	CHIPCAP X7R 33N M 50V	0805
C435	2310791	CHIPCAP X7R 33N M 50V	0805
C436	2320131	CHIPCAP X7R 33N K 16V	0603
C437	2320131	CHIPCAP X7R 33N K 16V	0603
C501	2320518	CHIPCAP NP0 1P8 C 50V	0402
C502	2320532	CHIPCAP NP0 6P8 C 50V	0402
C503	2320560	CHIPCAP NP0 100P J 50V	0402
C504	2320536	CHIPCAP NP0 10P J 50V	0402
C505	2320544	CHIPCAP NP0 22P J 50V	0402
C506	2320516	CHIPCAP NP0 1P5 C 50V	0402
C508	2320756	CHIPCAP X7R 3N3 K 50V	0402
C509	2320544	CHIPCAP NP0 22P J 50V	0402
C510	2320544	CHIPCAP NP0 22P J 50V	0402
C511	2320604	CHIPCAP NP0 18P J 50V	0402
C512	2320518	CHIPCAP NP0 1P8 C 50V	0402
C513	2320516	CHIPCAP NP0 1P5 C 50V	0402
C514	2320516	CHIPCAP NP0 1P5 C 50V	0402
C515	2320756	CHIPCAP X7R 3N3 K 50V	0402
C516	2320560	CHIPCAP NP0 100P J 50V	0402
C517	2320548	CHIPCAP NP0 33P J 50V	0402
C521	2320524	CHIPCAP NP0 3P3 C 50V	0402
C522	2320744	CHIPCAP X7R 1N0 K 50V	0402
C523	2320550	CHIPCAP NP0 39P J 50V	0402
C524	2320544	CHIPCAP NP0 22P J 50V	0402

C525	2320544	CHIPCAP NP0 22P J 50V	0402
C526	2320604	CHIPCAP NP0 18P J 50V	0402
C527	2320544	CHIPCAP NP0 22P J 50V	0402
C528	2320526	CHIPCAP NP0 3P9 C 50V	0402
C529	2320532	CHIPCAP NP0 6P8 C 50V	0402
C530	2320604	CHIPCAP NP0 18P J 50V	0402
C531	2320520	CHIPCAP NP0 2P2 C 50V	0402
C532	2320540	CHIPCAP NP0 15P J 50V	0402
C533	2320744	CHIPCAP X7R 1N0 K 50V	0402
C534	2320756	CHIPCAP X7R 3N3 K 50V	0402
C535	2320532	CHIPCAP NP0 6P8 C 50V	0402
C536	2320554	CHIPCAP NP0 56P J 50V	0402
C537	2320604	CHIPCAP NP0 18P J 50V	0402
C538	2320534	CHIPCAP NP0 8P2 C 50V	0402
C541	2320756	CHIPCAP X7R 3N3 K 50V	0402
C542	2320744	CHIPCAP X7R 1N0 K 50V	0402
C543	2320756	CHIPCAP X7R 3N3 K 50V	0402
C544	2320744	CHIPCAP X7R 1N0 K 50V	0402
C545	2320560	CHIPCAP NP0 100P J 50V	0402
C546	2320560	CHIPCAP NP0 100P J 50V	0402
C547	2320544	CHIPCAP NP0 22P J 50V	0402
C551	2320534	CHIPCAP NP0 8P2 C 50V	0402
C552	2320560	CHIPCAP NP0 100P J 50V	0402
C553	2320560	CHIPCAP NP0 100P J 50V	0402
C554	2320564	CHIPCAP NP0 150P J 50V	0402
C555	2320564	CHIPCAP NP0 150P J 50V	0402
C556	2320752	CHIPCAP X7R 2N2 K 50V	0402
C557	2320560	CHIPCAP NP0 100P J 50V	0402
C558	2320560	CHIPCAP NP0 100P J 50V	0402
C559	2320752	CHIPCAP X7R 2N2 K 50V	0402
C560	2320752	CHIPCAP X7R 2N2 K 50V	0402
C561	2320560	CHIPCAP NP0 100P J 50V	0402
C562	2320075	CHIPCAP X7R 470P J 50V	0603
C563	2320578	CHIPCAP X7R 560P J 50V	0402
C564	2320560	CHIPCAP NP0 100P J 50V	0402
C565	2310470	CHIPCAP NP0 270P J 50V	0805
C566	2320558	CHIPCAP NP0 82P J 50V	0402
C567	2310470	CHIPCAP NP0 270P J 50V	0805
C569	2320756	CHIPCAP X7R 3N3 K 50V	0402
C570	2320756	CHIPCAP X7R 3N3 K 50V	0402
C571	2320756	CHIPCAP X7R 3N3 K 50V	0402
C572	2310791	CHIPCAP X7R 33N M 50V	0805

C573	2320560	CHIPCAP NP0 100P J 50V	0402
C574	2320560	CHIPCAP NP0 100P J 50V	0402
C575	2320530	CHIPCAP NP0 5P6 C 50V	0402
C580	2320744	CHIPCAP X7R 1N0 K 50V	0402
C581	2320516	CHIPCAP NP0 1P5 C 50V	0402
C582	2320516	CHIPCAP NP0 1P5 C 50V	0402
C601	2310784	CHIPCAP X7R 100N K 25V	0805
C602	2312410	CHIPCAP X5R 1U0 K 16V	1206
C603	2312410	CHIPCAP X5R 1U0 K 16V	1206
C604	2310784	CHIPCAP X7R 100N K 25V	0805
C605	2312410	CHIPCAP X5R 1U0 K 16V	1206
C606	2310791	CHIPCAP X7R 33N M 50V	0805
C607	2310784	CHIPCAP X7R 100N K 25V	0805
C608	2310784	CHIPCAP X7R 100N K 25V	0805
C609	2310784	CHIPCAP X7R 100N K 25V	0805
C701	2320548	CHIPCAP NP0 33P J 50V	0402
C702	2320560	CHIPCAP NP0 100P J 50V	0402
C703	2320756	CHIPCAP X7R 3N3 K 50V	0402
C704	2320516	CHIPCAP NP0 1P5 C 50V	0402
C705	2320514	CHIPCAP NP0 1P2 C 50V	0402
C710	2320744	CHIPCAP X7R 1N0 K 50V	0402
C711	2320536	CHIPCAP NP0 10P J 50V	0402
C712	2320522	CHIPCAP NP0 2P7 C 50V	0402
C714	2320534	CHIPCAP NP0 8P2 C 50V	0402
C715	2320522	CHIPCAP NP0 2P7 C 50V	0402
C717	2320524	CHIPCAP NP0 3P3 C 50V	0402
C718	2320518	CHIPCAP NP0 1P8 C 50V	0402
C720	2320544	CHIPCAP NP0 22P J 50V	0402
C721	2320744	CHIPCAP X7R 1N0 K 50V	0402
C725	2320544	CHIPCAP NP0 22P J 50V	0402
C726	2320516	CHIPCAP NP0 1P5 C 50V	0402
C727	2320560	CHIPCAP NP0 100P J 50V	0402
C729	2320524	CHIPCAP NP0 3P3 C 50V	0402
C730	2320544	CHIPCAP NP0 22P J 50V	0402
C735	2320526	CHIPCAP NP0 3P9 C 50V	0402
C736	2320516	CHIPCAP NP0 1P5 C 50V	0402
C737	2320560	CHIPCAP NP0 100P J 50V	0402
C738	2320560	CHIPCAP NP0 100P J 50V	0402
C739	2320584	CHIPCAP X7R 1N0 J 50V	0402
C740	2320524	CHIPCAP NP0 3P3 C 50V	0402
C741	2320544	CHIPCAP NP0 22P J 50V	0402
C755	2320524	CHIPCAP NP0 3P3 C 50V	0402

C756	2320584	CHIPCAP X7R 1N0 J 50V	0402
C758	2320560	CHIPCAP NP0 100P J 50V	0402
C759	2320584	CHIPCAP X7R 1N0 J 50V	0402
C760	2320544	CHIPCAP NP0 22P J 50V	0402
C761	2320522	CHIPCAP NP0 2P7 C 50V	0402
C763	2610011	CHIPTCAP 330U K 10V	6.9X6X3.5
C765	2320584	CHIPCAP X7R 1N0 J 50V	0402
C766	2320522	CHIPCAP NP0 2P7 C 50V	0402
C767	2320578	CHIPCAP X7R 560P J 50V	0402
C768	2320554	CHIPCAP NP0 56P J 50V	0402
C769	2320584	CHIPCAP X7R 1N0 J 50V	0402
C770	2320584	CHIPCAP X7R 1N0 J 50V	0402
C771	2320536	CHIPCAP NP0 10P J 50V	0402
C772	2320524	CHIPCAP NP0 3P3 C 50V	0402
C774	2320530	CHIPCAP NP0 5P6 C 50V	0402
C775	2320518	CHIPCAP NP0 1P8 C 50V	0402
C776	2320508	CHIPCAP NP0 1P0 C 50V	0402
C780	2320536	CHIPCAP NP0 10P J 50V	0402
C781	2320536	CHIPCAP NP0 10P J 50V	0402
C782	2320546	CHIPCAP NP0 27P J 50V	0402
C783	2320546	CHIPCAP NP0 27P J 50V	0402
C784	2320756	CHIPCAP X7R 3N3 K 50V	0402
C791	2610200	CHIPTCAP 2U2 M 6V3	2.0X1.3X1.2
C793	2610200	CHIPTCAP 2U2 M 6V3	2.0X1.3X1.2
C794	2610200	CHIPTCAP 2U2 M 6V3	2.0X1.3X1.2
C795	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C796	2610011	CHIPTCAP 330U K 10V	6.9X6X3.5
C797	2610011	CHIPTCAP 330U K 10V	6.9X6X3.5
C798	2610011	CHIPTCAP 330U K 10V	6.9X6X3.5
C799	2610011	CHIPTCAP 330U K 10V	6.9X6X3.5
C800	2604079	CHIPTCAP 0U22 M 35V	3.2X1.6X1.6
C801	2310791	CHIPCAP X7R 33N M 50V	0805
C803	2320568	CHIPCAP X7R 220P J 50V	0402
C804	2320552	CHIPCAP NP0 47P J 50V	0402
C805	2320728	CHIPCAP X7R 220P K 50V	0402
C806	2610100	CHIPTCAP 1U M 10V	2.0X1.3X1.2
C807	2320756	CHIPCAP X7R 3N3 K 50V	0402
C808	2320756	CHIPCAP X7R 3N3 K 50V	0402
C809	2320744	CHIPCAP X7R 1N0 K 50V	0402
C810	2320728	CHIPCAP X7R 220P K 50V	0402
C820	2320560	CHIPCAP NP0 100P J 50V	0402
C821	2310248	CHIPCAP NP0 4N7 J 50V	1206

C822	2320466	CHIPCAP NP0 220P J 50V 0603
C823	2310248	CHIPCAP NP0 4N7 J 50V 1206
C824	2320564	CHIPCAP NP0 150P J 50V 0402
C828	2610100	CHIPTCAP 1U M 10V 2.0X1.3X1.2
C829	2320756	CHIPCAP X7R 3N3 K 50V 0402
C830	2320560	CHIPCAP NP0 100P J 50V 0402
C831	2610100	CHIPTCAP 1U M 10V 2.0X1.3X1.2
C832	2320756	CHIPCAP X7R 3N3 K 50V 0402
C840	2320530	CHIPCAP NP0 5P6 C 50V 0402
C841	2610100	CHIPTCAP 1U M 10V 2.0X1.3X1.2
C842	2320584	CHIPCAP X7R 1N0 J 50V 0402
C843	2320544	CHIPCAP NP0 22P J 50V 0402
C844	2320536	CHIPCAP NP0 10P J 50V 0402
C845	2320536	CHIPCAP NP0 10P J 50V 0402
C846	2320536	CHIPCAP NP0 10P J 50V 0402
C847	2320520	CHIPCAP NP0 2P2 C 50V 0402
C848	2320560	CHIPCAP NP0 100P J 50V 0402
C849	2320744	CHIPCAP X7R 1N0 K 50V 0402
C850	2320534	CHIPCAP NP0 8P2 C 50V 0402
C851	2320534	CHIPCAP NP0 8P2 C 50V 0402
C862	2320602	CHIPCAP NP0 4P7 C 50V 0402
C864	2320560	CHIPCAP NP0 100P J 50V 0402
C865	2320560	CHIPCAP NP0 100P J 50V 0402
D300	4340126	TC7S00F 1XNAND 2INPUT CMOS SSO5
D301	4340126	TC7S00F 1XNAND 2INPUT CMOS SSO5
G300	4510044	SMCRYST 60.2MHZ+–50PPM7.3X4.9X1.1
L200	3641262	FERRITE BEAD 30R/100MHZ 2A 1206
L201	3606946	FERRITE BEAD 0.2R 26R/100MHZ 1206
L202	3641262	FERRITE BEAD 30R/100MHZ 2A 1206
L203	3641548	CHIP COIL 100N K Q40/150MHZ 0805
L230	3606946	FERRITE BEAD 0.2R 26R/100MHZ 1206
L231	3606946	FERRITE BEAD 0.2R 26R/100MHZ 1206
L232	3606946	FERRITE BEAD 0.2R 26R/100MHZ 1206
L300	3641302	CHIP COIL 470NH J Q30/25MHZ 1008
L511	3641546	CHIP COIL 82N K Q40/150MHZ 0805
L530	3641536	CHIP COIL 33N M Q40/250MHZ 0805
L531	3608414	CHIP COIL 560NH J 1206
L532	3641560	CHIP COIL 220N K Q30/100MHZ 0805
L541	3641550	CHIP COIL 120N K Q35/150MHZ 0805
L542	3608238	CHIP COIL 180NH K 1206
L543	3608319	CHIP COIL 270NH K 1206
L544	3608319	CHIP COIL 270NH K 1206

L545	3608238	CHIP COIL 180NH K 1206
L551	3641522	CHIP COIL 6N8 M Q50/250MHZ 0805
L700	3606946	FERRITE BEAD 0.2R 26R/100MHZ 1206
L710	3641536	CHIP COIL 33N M Q40/250MHZ 0805
L711	3641536	CHIP COIL 33N M Q40/250MHZ 0805
L800	3641206	CHIP COIL 3U3 K Q25/7.96MHZ 1008
L801	3641206	CHIP COIL 3U3 K Q25/7.96MHZ 1008
L840	3641572	CHIP COIL 22N J Q45/250MHZ 0805
L841	3641522	CHIP COIL 6N8 M Q50/250MHZ 0805
N230	4375588	PSL+ POWER SUPPLY VERSION D SO24W
N400	4340303	LM4861 AF AMP 0.5W 2.7–5.5V SO8S
N551	4370091	CRFRT_ST TX.MOD+RXIF+PWC SQFP44
N601	4370095	CRFCONTF 8XREG4.5V VREF2V5 VSOP28
N790	4349576	ICL7660 V.CONV+1.5–12VTO NEG SO8
N820	4340021	LMX2331 2XSYNTH 2G/510MHZ SSO20
T300	3640402	TRANSFORMER 4:1 BALUN 800MHZ SMD
V200	4111824	DI BAS16 75V 250MA 6NS SOT23
V201	4111824	DI BAS16 75V 250MA 6NS SOT23
V202	4100285	DIX2 BAV99 70V 200MA IN SER.SOT23
V230	4210020	TR BCP69–25 P 20V 1A >160 SOT223
V231	4200877	TR BCX51–16 P 45V 1.5A 1W SOT89
V232	4210020	TR BCP69–25 P 20V 1A >160 SOT223
V250	4210020	TR BCP69–25 P 20V 1A >160 SOT223
V251	4110074	SCH DI STPS340U 40V 3A SOD6
V253	4200226	TR BCV27 N 30V 300MA DARL SOT23
V254	4200226	TR BCV27 N 30V 300MA DARL SOT23
V255	4200909	TR BC858B/BCW30 P 30V 100MA SOT23
V256	4110126	ZDI BZX84 4.3V 5% 0.3W SOT23
V257	4202671	FET BST82 N 80V 175MA 7R SOT23
V300	4210079	TR BFS17 N 15V 50MA 1.3GHZ SOT23
V301	4210079	TR BFS17 N 15V 50MA 1.3GHZ SOT23
V302	4210050	TR DTA114EE P RB=RBE=10K EM3
V303	4210100	TR BC848W N 30V 0.1A100MHZ SOT323
V320	4110014	SCHDIX2 BAS70–07 70V 15MA SOT143
V330	4210100	TR BC848W N 30V 0.1A100MHZ SOT323
V331	4200909	TR BC858B/BCW30 P 30V 100MA SOT23
V370	4210102	TR BC858W P 30V 100MA 200MWSOT323
V380	4200829	TR BC859C P 30V 0.1A SOT23
V381	4200811	TR BC849C N 30V 0.1A SOT23
V400	4200917	TR BC848B/BCW32 N 30V 100MA SOT23
V420	4117998	PRECISION VOLTAGE REFERENCE 4.096
V460	4110014	SCHDIX2 BAS70–07 70V 15MA SOT143

V501	4210046	TR BFP182 N 20V 35MA 8GHZ SOT143
V502	4210102	TR BC858W P 30V 100MA 200MWSOT323
V503	4210100	TR BC848W N 30V 0.1A100MHZ SOT323
V504	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V511	4115802	SCH DIX2 4V 30MA <1PF SER SOT23
V512	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V521	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V531	4100567	SCHDIX2 BAS70–04 70V15MA SERSOT23
V532	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V541	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V701	4210058	TR MRF947 N 10V 50MA 8GHZ SOT323
V702	4100567	SCHDIX2 BAS70–04 70V15MA SERSOT23
V710	4210046	TR BFP182 N 20V 35MA 8GHZ SOT143
V725	4210074	TR BFP420 N 4.5V35MA 20GHZ SOT343
V726	4210102	TR BC858W P 30V 100MA 200MWSOT323
V735	4217070	TRX2 IMZ1 N&P ISOLATED IMD
V736	4210090	TR BFG540/X N 15V 129MA 9G SOT143
V737	4210100	TR BC848W N 30V 0.1A100MHZ SOT323
V738	4210020	TR BCP69–25 P 20V 1A >160 SOT223
V739	4217070	TRX2 IMZ1 N&P ISOLATED IMD
V740	4210102	TR BC858W P 30V 100MA 200MWSOT323
V741	4210100	TR BC848W N 30V 0.1A100MHZ SOT323
V755	4210102	TR BC858W P 30V 100MA 200MWSOT323
V756	4210343	FET GAAS CLY2 9V 0.6A 3GHZ MW6
V765	4211485	FET GAAS N 6V2A 1.8GHZ33DBM SOT89
V766	4219908	TRX2 UMT1 P 40V 0.1A140MHZ SOT363
V780	4110014	SCHDIX2 BAS70–07 70V 15MA SOT143
V790	4100285	DIX2 BAV99 70V 200MA IN SER.SOT23
V791	4210102	TR BC858W P 30V 100MA 200MWSOT323
V792	4107040	ZDI BZX84 6.2V 5% 0.3W SOT23
V800	4110081	CAP.DI BB640 3/62PF 28/1V SOD323
V801	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V802	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V840	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V841	4210066	TR BFR93AW N 12V 35MA 5GHZ SOT323
V842	4110018	CAP.DI BB135 30V 2.1/21PF SOD323
X201	5469203	SM CONN 2X22 F P0.8 PCB/PCB 9.0MM
X202	5409041	SM CONN BATTERY 4POL P2.54
X212	5469037	SM FLEX CONN 12POL P0.5 U.CONTACT
X400	5469031	SM CONN CHP2502–0101 1X2 M P1.25
X501	5429003	SM COAX CONN RECEP 50R 3GHZ 5X4.5
X503	5420460	COAX–CONN FEMALE 50OHM SWITCH IMS

Z500	4512047	DUPL 1710–1785/1805–1880MHZ 31X12
Z505	4550105	CER.FILT 1842.5+–37.5MHZ 8.9X4.8
Z541	4511028	SAW FILT 87+–0.12MHZ/13DB14.2X8.4
Z551	4510009	CER.FILT 13+–0.09MHZ 330R 7.3X3.3
Z713	4550103	CER.FILT 1747.5+–37.5MHZ 8.9X5
Z727	4550103	CER.FILT 1747.5+–37.5MHZ 8.9X5
	9854163	PCB GE9 121.0X55.0X1.0 M6 2/PA
	4510071	SMCRYST 26.000MHZ+–7/TSTAB+–10PPM
MCM1	0200865	SUBMODULE
MCM2	0200726	SUBMODULE

PDA Module – GP1

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Item	Code	Description	Value	Type
R065	1430822	Chip resistor	560 k	5 % 0.063 W 0402
R072	1430830	Chip resistor	1.0 M	5 % 0.063 W 0402
R074	1430142	Chip resistor	4.7	5 % 0.063 W 0603
R075	1430830	Chip resistor	1.0 M	5 % 0.063 W 0402
R076	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R077	1430700	Chip resistor	10	5 % 0.063 W 0402
R078	1430183	Chip resistor	110 k	1 % 0.063 W 0603
R080	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R081	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R082	1430113	Chip resistor	348 k	1 % 0.063 W 0603
R083	1430822	Chip resistor	560 k	5 % 0.063 W 0402
R084	1430181	Chip resistor	30.9 k	1 % 0.063 W 0603
R085	1430142	Chip resistor	4.7	5 % 0.063 W 0603
R086	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R087	1414526	Chip resistor	120 k	1 % 0.1 W 0805
R088	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R089	1430131	Chip resistor	464 k	1 % 0.063 W 0603
R090	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R092	1430820	Chip resistor	470 k	5 % 0.063 W 0402
R093	1820026	NTC resistor	100 k	5 % 0805
R094	1430830	Chip resistor	1.0 M	5 % 0.063 W 0402
R095	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R096	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R097	1820026	NTC resistor	100 k	5 % 0805
R098	1430820	Chip resistor	470 k	5 % 0.063 W 0402
R112	1430746	Chip resistor	560	5 % 0.063 W 0402
R113	1430746	Chip resistor	560	5 % 0.063 W 0402
R114	1430746	Chip resistor	560	5 % 0.063 W 0402
R115	1430746	Chip resistor	560	5 % 0.063 W 0402
R116	1430746	Chip resistor	560	5 % 0.063 W 0402
R117	1430746	Chip resistor	560	5 % 0.063 W 0402
R118	1430746	Chip resistor	560	5 % 0.063 W 0402
R119	1430746	Chip resistor	560	5 % 0.063 W 0402
R120	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R121	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R122	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R123	1430788	Chip resistor	22 k	5 % 0.063 W 0402

R124	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R125	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R126	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R127	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R128	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R129	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R130	1430800	Chip resistor	68 k	5 % 0.063 W 0402
R131	1430800	Chip resistor	68 k	5 % 0.063 W 0402
R132	1430800	Chip resistor	68 k	5 % 0.063 W 0402
R134	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R135	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R136	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R137	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R138	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R139	1430802	Chip resistor	82 k	5 % 0.063 W 0402
R140	1430135	Chip resistor	10 M	5 % 0.063 W 0603
R141	1430135	Chip resistor	10 M	5 % 0.063 W 0603
R143	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R145	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R146	1430135	Chip resistor	10 M	5 % 0.063 W 0603
R147	1430834	Chip resistor	3.3 M	5 % 0.063 W 0402
R148	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R150	1430726	Chip resistor	100	5 % 0.063 W 0402
R151	1430726	Chip resistor	100	5 % 0.063 W 0402
R175	1430015	Chip resistor	470	5 % 0.063 W 0603
R176	1411282	Chip resistor	4.7	5 % 0.12 W 1206
R177	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R180	1430714	Chip resistor	33	5 % 0.063 W 0402
R181	1430714	Chip resistor	33	5 % 0.063 W 0402
R182	1430714	Chip resistor	33	5 % 0.063 W 0402
R183	1430714	Chip resistor	33	5 % 0.063 W 0402
R184	1430714	Chip resistor	33	5 % 0.063 W 0402
R185	1430714	Chip resistor	33	5 % 0.063 W 0402
R186	1430714	Chip resistor	33	5 % 0.063 W 0402
R187	1430714	Chip resistor	33	5 % 0.063 W 0402
R188	1430714	Chip resistor	33	5 % 0.063 W 0402
R189	1430714	Chip resistor	33	5 % 0.063 W 0402
R192	1430714	Chip resistor	33	5 % 0.063 W 0402
R193	1430714	Chip resistor	33	5 % 0.063 W 0402
R194	1430714	Chip resistor	33	5 % 0.063 W 0402
R195	1430714	Chip resistor	33	5 % 0.063 W 0402
R900	1430726	Chip resistor	100	5 % 0.063 W 0402

R901	1430722	Chip resistor	68	5 % 0.063 W 0402
R902	1430726	Chip resistor	100	5 % 0.063 W 0402
R903	1430722	Chip resistor	68	5 % 0.063 W 0402
R904	1430726	Chip resistor	100	5 % 0.063 W 0402
R905	1430722	Chip resistor	68	5 % 0.063 W 0402
R906	1430726	Chip resistor	100	5 % 0.063 W 0402
R907	1430722	Chip resistor	68	5 % 0.063 W 0402
R908	1430726	Chip resistor	100	5 % 0.063 W 0402
R909	1430722	Chip resistor	68	5 % 0.063 W 0402
R910	1430726	Chip resistor	100	5 % 0.063 W 0402
R911	1430722	Chip resistor	68	5 % 0.063 W 0402
R912	1430726	Chip resistor	100	5 % 0.063 W 0402
R913	1430722	Chip resistor	68	5 % 0.063 W 0402
R914	1430726	Chip resistor	100	5 % 0.063 W 0402
R915	1430722	Chip resistor	68	5 % 0.063 W 0402
R916	1430726	Chip resistor	100	5 % 0.063 W 0402
R917	1430722	Chip resistor	68	5 % 0.063 W 0402
R922	1430726	Chip resistor	100	5 % 0.063 W 0402
R923	1430726	Chip resistor	100	5 % 0.063 W 0402
R924	1430726	Chip resistor	100	5 % 0.063 W 0402
R925	1430726	Chip resistor	100	5 % 0.063 W 0402
R926	1430726	Chip resistor	100	5 % 0.063 W 0402
R927	1430722	Chip resistor	68	5 % 0.063 W 0402
R928	1430726	Chip resistor	100	5 % 0.063 W 0402
R929	1430726	Chip resistor	100	5 % 0.063 W 0402
R930	1430726	Chip resistor	100	5 % 0.063 W 0402
R931	1430726	Chip resistor	100	5 % 0.063 W 0402
R932	1430726	Chip resistor	100	5 % 0.063 W 0402
R933	1430722	Chip resistor	68	5 % 0.063 W 0402
R936	1430714	Chip resistor	33	5 % 0.063 W 0402
R937	1430714	Chip resistor	33	5 % 0.063 W 0402
R938	1430726	Chip resistor	100	5 % 0.063 W 0402
R939	1430726	Chip resistor	100	5 % 0.063 W 0402
R940	1430726	Chip resistor	100	5 % 0.063 W 0402
R941	1430722	Chip resistor	68	5 % 0.063 W 0402
R942	1430726	Chip resistor	100	5 % 0.063 W 0402
R943	1430726	Chip resistor	100	5 % 0.063 W 0402
R944	1430726	Chip resistor	100	5 % 0.063 W 0402
R945	1430726	Chip resistor	100	5 % 0.063 W 0402
R948	1430726	Chip resistor	100	5 % 0.063 W 0402
R949	1430726	Chip resistor	100	5 % 0.063 W 0402
R950	1430726	Chip resistor	100	5 % 0.063 W 0402

R951	1430726	Chip resistor	100	5 % 0.063 W 0402	
R952	1430726	Chip resistor	100	5 % 0.063 W 0402	
R953	1430726	Chip resistor	100	5 % 0.063 W 0402	
R954	1430726	Chip resistor	100	5 % 0.063 W 0402	
R955	1430726	Chip resistor	100	5 % 0.063 W 0402	
R956	1430726	Chip resistor	100	5 % 0.063 W 0402	
R970	1430726	Chip resistor	100	5 % 0.063 W 0402	
R971	1430726	Chip resistor	100	5 % 0.063 W 0402	
R972	1430726	Chip resistor	100	5 % 0.063 W 0402	
R973	1430726	Chip resistor	100	5 % 0.063 W 0402	
R974	1430788	Chip resistor	22 k	5 % 0.063 W 0402	
R975	1825001	Chip varistor vwm18v vc40v		0603	0603
R976	1825001	Chip varistor vwm18v vc40v		0603	0603
R980	1825001	Chip varistor vwm18v vc40v		0603	0603
R982	1825001	Chip varistor vwm18v vc40v		0603	0603
R983	1825001	Chip varistor vwm18v vc40v		0603	0603
R984	1430726	Chip resistor	100	5 % 0.063 W 0402	
R985	1430726	Chip resistor	100	5 % 0.063 W 0402	
R986	1825001	Chip varistor vwm18v vc40v		0603	0603
R987	1430752	Chip resistor	820	5 % 0.063 W 0402	
C068	2320544	Ceramic cap.	22 p	5 % 50 V 0402	
C069	2320544	Ceramic cap.	22 p	5 % 50 V 0402	
C079	2320544	Ceramic cap.	22 p	5 % 50 V 0402	
C080	2610009	Tantalum cap.	1.5 u	20 %	
C081	2604431	Tantalum cap.	10 u	20 % 16 V 6.0x3.2x2.5	
C082	2310495	Ceramic cap.	390 p	5 % 50 V 0805	
C083	2610103	Tantalum cap.	100 u	20 % 16 V 7.3x4.3x4.1	
C084	2610105	Tantalum cap.	100 u	20 % 10 V 7.3x4.3x2.9	
C085	2320120	Ceramic cap.	22 n	10 % 25 V 0603	
C086	2310784	Ceramic cap.	100 n	10 % 25 V 0805	
C087	2310784	Ceramic cap.	100 n	10 % 25 V 0805	
C088	2310784	Ceramic cap.	100 n	10 % 25 V 0805	
C089	2610109	Tantalum cap.	22 u	20 % 25 V 7.3x4.3x2.9	
C090	2320107	Ceramic cap.	10 n	5 % 50 V 0603	
C091	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402	
C093	2320107	Ceramic cap.	10 n	5 % 50 V 0603	
C094	2320107	Ceramic cap.	10 n	5 % 50 V 0603	
C095	2320107	Ceramic cap.	10 n	5 % 50 V 0603	
C096	2310784	Ceramic cap.	100 n	10 % 25 V 0805	
C097	2320107	Ceramic cap.	10 n	5 % 50 V 0603	
C098	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402	
C099	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402	

C130	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C131	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C132	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C133	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C134	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C135	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C136	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C137	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C139	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C140	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C141	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C142	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C143	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C144	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C147	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C148	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C149	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C150	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C151	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C152	2320120	Ceramic cap.	22 n	10 % 25 V 0603
C153	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C154	2320120	Ceramic cap.	22 n	10 % 25 V 0603
C155	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C156	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C157	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C158	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C159	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C160	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C161	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C162	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C163	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C164	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C165	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C166	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C167	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C180	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C181	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C182	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C183	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C184	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C185	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C900	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C901	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C902	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C903	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C904	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C905	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C906	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C907	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C908	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C911	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C912	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C913	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C914	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C915	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C916	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C917	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C918	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C920	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C921	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C922	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C923	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C924	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C926	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C927	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C928	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C929	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C930	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C931	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C933	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C970	2310752	Ceramic cap.	10 n	20 % 50 V 0805
C971	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C972	2320560	Ceramic cap.	100 p	5 % 50 V 0402
L080	3640025	Chip coil		20 % 500 mA Q=30/1M 1812
L081	3640019	Chip coil 56 u		10 % 200 mA Q=35 1812
L082	3640027	Chip coil 22 u		20 % 0.81 A 6.2x6.6x3
L970	3606946	Ferrite bead 0.2r 26r/100mhz 1206		
B130	4510003	Crystal 32.768 k		+–20PPM 8x3.8
G087	4700029	Battery cr2320 li 3v 130mah d23x2		
Z130	3640021	Filt z>60r/100m 0r2max 0.5a 0603		
Z131	3640021	Filt z>60r/100m 0r2max 0.5a 0603		
V080	4211264	MosFet 2SJ16		SOT23
V081	4202671	MosFet BST82		n–ch 80 V 175 mA SOT23
V082	4211264	MosFet 2SJ16		SOT23

V084	4117998	Precision voltage reference 4.096			
V085	4100189	Schottky diode BAS 70–05 70V 15mA SOT23			
V086	4210100	Transistor BC848W	npn 30V SOT323		
V087	4210100	Transistor BC848W	npn 30V SOT323		
V088	4110063	Schottky diode	MBRS140	DO214AA	
V089	4111853	Diode LS4150	50V 600mA 4 ns QMELF		
V130	4200226	Darl. transistor	BCV27	npn 30V 300mA SOT23	
V131	4110078	Schdix2 bas70–05w 70v 70ma sot323			SOT323
V135	4200226	Darl. transistor	BCV27	npn 30V 300mA SOT23	
V970	4110028	Trans. supr.	16V	23A 600W DO214AA	
D080	4340121	Max809t mcu reset/3.08v	SOT23		
D130	4370135	IC, MCU	TQFP176		
D160	4340111	Dram 1mx16bit 60ns 3v3		TS0P2/44	
D161	4340207	IC, 1mx16bit120ns 3.3v tsop	E28F016	TSOP56	
D162	4340205	IC, flash memory	E28F016SV	TSOP56	
D163	4340205	IC, flash memory	E28F016SV	TSOP56	
D180	4340091	Max3222 4xrs232 transceiver		VSO20	
N080	4340113	IC, regulator	LP2980IM5X–5.0	5V 50mA SOT23	
N081	4340129	Max763a sw reg 3.3v 0.5 a 5% so8s			SO8S
N082	4340123	IC, 2 x comp.	LMC6762 SO8S		
N083	4340109	Max772 sw reg 2–16.5v max 1a so8s			SO8S
N180	4860013	Tfds3020 irda sir ir tx/rx sm8pin			SM8PIN
S170	5308940	Reed relay 1a 10–25at 0.5a 2.5x1			2.5x10
X101	5449506	Pin header 1x02 1.25mm angle smd			SMD
X102	5469207	SM, conn 2x22 m p0.8 pcb/pcb 9.0			9.0MM
X110	5469019	SM, flex conn sfv 33pol p0.5 u.c			U.CON
X121	5469017	SM, system conn 12pol m p1.27			
	9854108	PCB GP1 170.9X51.0X1.0 M8 2/PA			

User Interface – GK2

EDMS pn 0200708 issue 3.0

Item	Code	Description	Value	Type
R001	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R002	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R003	1430075	Chip resistor	33 k	5 % 0.063 W 0603
R004	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R005	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R006	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R007	1430057	Chip resistor	8.2 k	5 % 0.063 W 0603
R008	1430076	Chip resistor	36 k	5 % 0.063 W 0603
R010	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R011	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R012	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R013	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R014	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R015	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R016	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R017	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R018	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R019	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R020	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R021	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R022	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R030	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R031	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R032	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R033	1430165	Chip resistor	39	5 % 0.063 W 0603
R034	1430165	Chip resistor	39	5 % 0.063 W 0603
R035	1430165	Chip resistor	39	5 % 0.063 W 0603
R036	1430165	Chip resistor	39	5 % 0.063 W 0603
C001	2604248	Tantalum cap.	4.7 u	20 % 16 V 6.0x3.2x2.5
C002	2604248	Tantalum cap.	4.7 u	20 % 16 V 6.0x3.2x2.5
C003	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C004	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C005	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C006	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C007	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C008	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C009	2307816	Ceramic cap.	47 n	20 % 25 V 0805

C010	2604431	Tantalum cap.	10 u	20 % 16 V 6.0x3.2x2.5
C011	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C023	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C025	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C026	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C027	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C028	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C029	2310375	Ceramic cap.	39 p	5 % 50 V 0805
L001	3641520	Chip coil	3 n	20 % Q=50/250 MHz 0805
L002	3640013	Chip coil	8 n	5 % Q=50/250 MHz 0805
V011	4864388	Led	Green	0603
V012	4864388	Led	Green	0603
V013	4864388	Led	Green	0603
V014	4864388	Led	Green	0603
V015	4864388	Led	Green	0603
V016	4864388	Led	Green	0603
V017	4864388	Led	Green	0603
V018	4864388	Led	Green	0603
V019	4864388	Led	Green	0603
V020	4864388	Led	Green	0603
V021	4864388	Led	Green	0603
V022	4864388	Led	Green	0603
V023	4864388	Led	Green	0603
V024	4864388	Led	Green	0603
V026	4864388	Led	Green	0603
V027	4864388	Led	Green	0603
V028	4864388	Led	Green	0603
V029	4864388	Led	Green	0603
V030	4864388	Led	Green	0603
V031	4864388	Led	Green	0603
V032	4864388	Led	Green	0603
V033	4864388	Led	Green	0603
V034	4864388	Led	Green	0603
V036	4111824	Diode	BAS16	75 V 250 mA 6 ns SOT23
V038	4864388	Led	Green	0603
V040	4200811	Transistor	BC849C	npn 30 V 0.1 A SOT23
V041	4200836	Transistor	BCX19	npn 50 V 0.5 A SOT23
V042	4200836	Transistor	BCX19	npn 50 V 0.5 A SOT23
V043	4200836	Transistor	BCX19	npn 50 V 0.5 A SOT23
V044	4200836	Transistor	BCX19	npn 50 V 0.5 A SOT23
S036	5200120	Push button switch 6.4x5.2 smd		
X001	5469021	SM, flex conn		

X010	5469015	SM, flex conn sfv 12pol p0.5 loc	LOCK
X035	5429003	SM, coax conn recep 50r 3ghz 5x4	5x4.5
X040	9510168	Antenna contact b11114	
	4850038	IC, lcd 42dotm 3x7sgm 57ind DSL–12 EU	
	9457468	Lightguide rae–1 dmc00310	
	9795025	Keydome diam 5.6x20/sheet rae–1	RAE–1
	9854109	PCB GK2 165X51X0.6 M4 2/PA	
	9854109	PC board GK2 165x51x0.6 m4 2/pa	

User Interface – GK2–1

EDMS pn 0201034 issue 2.1

Item	Code	Description	Value	Type
R031	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R030	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R021	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R022	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R007	1430057	Chip resistor	8.2 k	5 % 0.063 W 0603
R001	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R002	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R004	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R005	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R010	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R011	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R012	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R013	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R014	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R003	1430075	Chip resistor	33 k	5 % 0.063 W 0603
R008	1430076	Chip resistor	36 k	5 % 0.063 W 0603
R006	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R015	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R016	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R017	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R018	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R019	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R020	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R032	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R033	1430165	Chip resistor	39	5 % 0.063 W 0603
R034	1430165	Chip resistor	39	5 % 0.063 W 0603
R035	1430165	Chip resistor	39	5 % 0.063 W 0603
R036	1430165	Chip resistor	39	5 % 0.063 W 0603
C003	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C004	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C005	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C006	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C007	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C008	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C009	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C029	2310375	Ceramic cap.	39 p	5 % 50 V 0805
C025	2320043	Ceramic cap.	22 p	5 % 50 V 0603

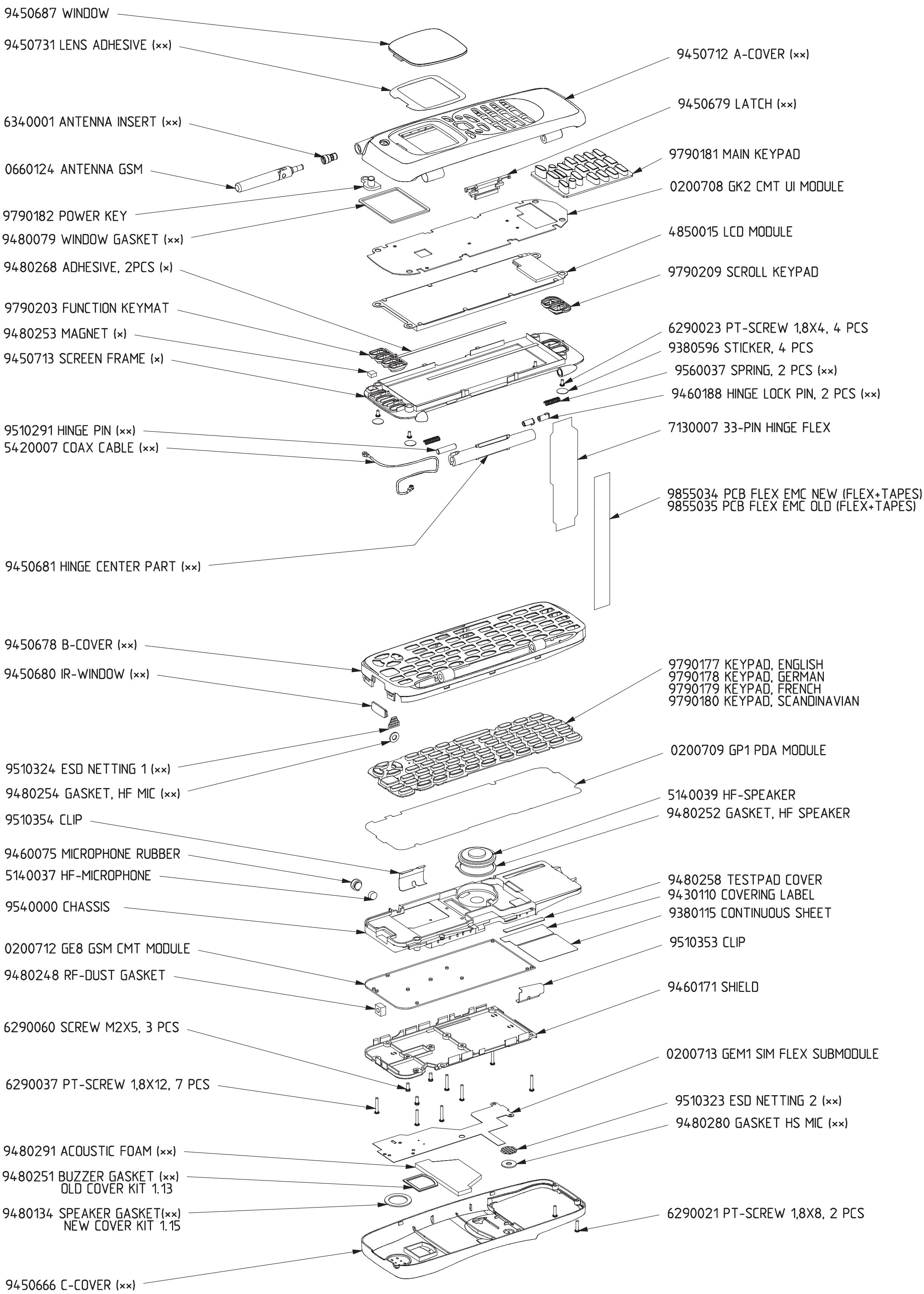
C026	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C027	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C028	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C011	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C001	2604248	Tantalum cap.	4.7 u	20 % 16 V 6.0x3.2x2.5
C002	2604248	Tantalum cap.	4.7 u	20 % 16 V 6.0x3.2x2.5
C010	2604431	Tantalum cap.	10 u	20 % 16 V 6.0x3.2x2.5
L002	3643041	Chip coil	2 n 7 +0N2 Q=42/450M 0805	
L001	3643043	Chip coil	3 n 3 +0N2 Q=38/450M 0805	
V036	4111824	Diode BAS16	75 V 250 mA 6 ns SOT23	
V040	4200811	Transistor BC849C	npn 30 V 0.1 A SOT23	
V041	4200836	Transistor BCX19	npn 50 V 0.5 A SOT23	
V042	4200836	Transistor BCX19	npn 50 V 0.5 A SOT23	
V043	4200836	Transistor BCX19	npn 50 V 0.5 A SOT23	
V044	4200836	Transistor BCX19	npn 50 V 0.5 A SOT23	
	4850038	IC, lcd 42dotm 3x7sgm 57ind		DSL–12 EU
V011	4864388	Led Green	0603	
V012	4864388	Led Green	0603	
V013	4864388	Led Green	0603	
V014	4864388	Led Green	0603	
V015	4864388	Led Green	0603	
V016	4864388	Led Green	0603	
V017	4864388	Led Green	0603	
V018	4864388	Led Green	0603	
V019	4864388	Led Green	0603	
V020	4864388	Led Green	0603	
V021	4864388	Led Green	0603	
V022	4864388	Led Green	0603	
V023	4864388	Led Green	0603	
V024	4864388	Led Green	0603	
V026	4864388	Led Green	0603	
V027	4864388	Led Green	0603	
V028	4864388	Led Green	0603	
V029	4864388	Led Green	0603	
V030	4864388	Led Green	0603	
V031	4864388	Led Green	0603	
V032	4864388	Led Green	0603	
V033	4864388	Led Green	0603	
V034	4864388	Led Green	0603	
V038	4864388	Led Green	0603	
S036	5200120	Push button switch 6.4x5.2 smd		
X035	5429003	SM, coax conn recep 50r 3ghz 5x4		5x4.5

X010	5469015	SM, flex conn sfv 12pol p0.5 loc	LOCK
X001	5469021	SM, flex conn 33pol po.5 l.conta	L.CONTACT
	9457468	Lightguide rae–1 dmc00310	
X040	9510168	Antenna contact b11114	
	9795025	Keydome diam 5.6x20/sheet rae–1	RAE–1
	9854198	PCB GK2–1 165.0X50.9X0.6 M4 2/PA	

Simflex Sub–module – GEM1

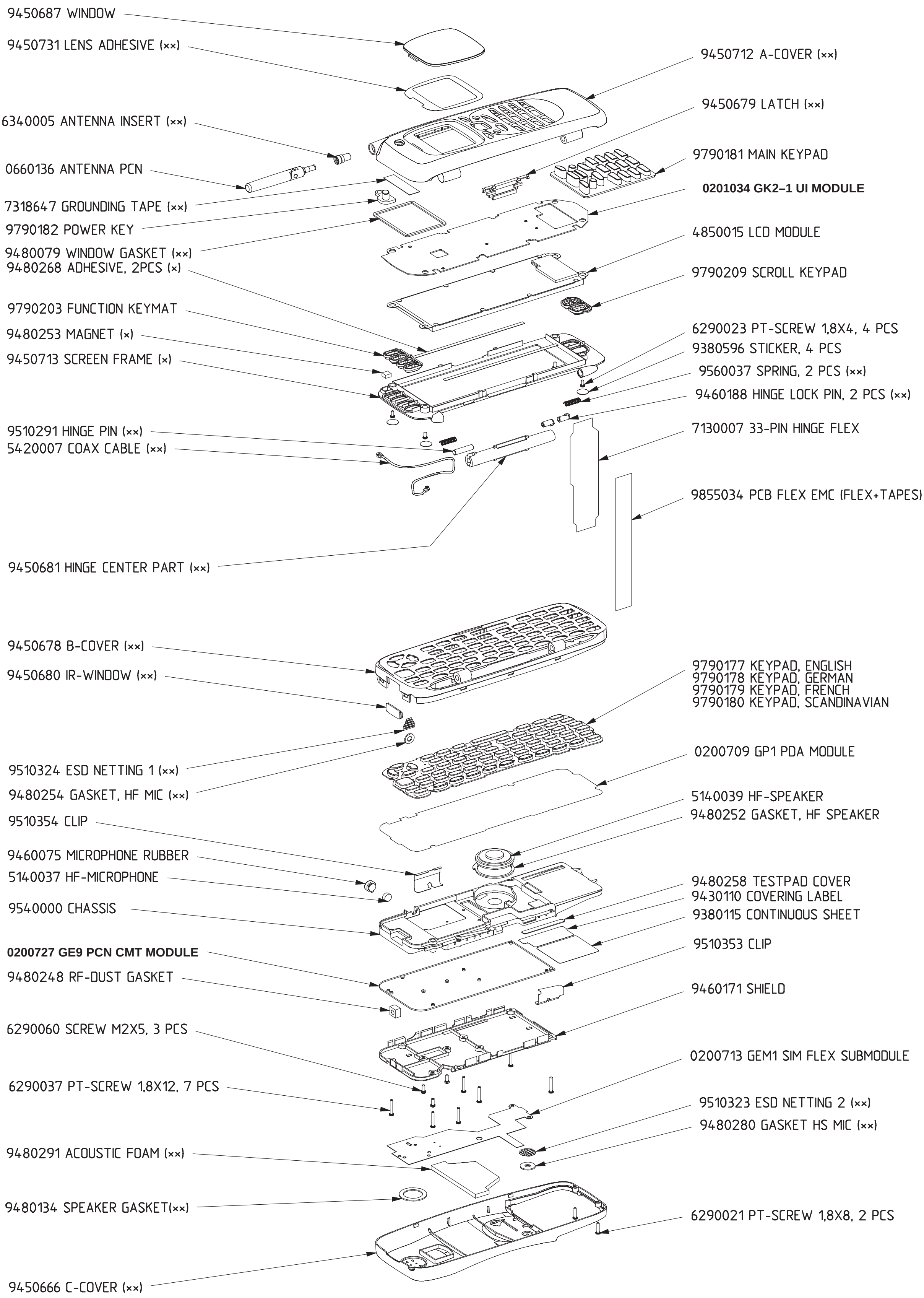
EDMS pn 0200713 issue 2.10

Item	Code	Description
B001	5140576	Dynamic receiver 32r
B002	5140458	Mic+wire 61.5+–2db1khz/2k/3v d6x3
B003	5140029	SM, d buzzer 94db 5vdc40r
X002	5409039	SM, sim card conn. 2x3+fix. hole
	7310007	Esd tape dmd00741
	9460100	Mic boot b10538
	9480103	Speaker pad2
	9854120	FLEX PCB GEM1



(×) 9450685 SCREEN FRAME SUBASSEMBLY
(××) 9480266 COVER KIT SUBASSEMBLY

Mechanical Assy/Parts RAE–1N



Mechanical Assy/Parts RAK–1N

(×) 9450685 SCREEN FRAME SUBASSEMBLY
(××) 9480343 PCN COVER KIT SUBASSEMBLY

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After Sales Technical Documentation
Appendix 1 RAE/RAK–1N

QUICK GUIDE

Original, 08/96

Contents

List of Figures

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Overview

The NOKIA 9000 Communicator has two interfaces, the phone interface and the communicator interface. The word “interface” emphasizes the fact that of these two aspects of the NOKIA 9000 Communicator both use the same resources and work closely together — **they are not separate devices.** For example, the phone interface uses names and phone numbers stored in the communicator interface’s Contacts directory and the communicator interface uses the phone interface for communicating with the “outside world”, for example, sending, receiving faxes and connecting to remote computers.

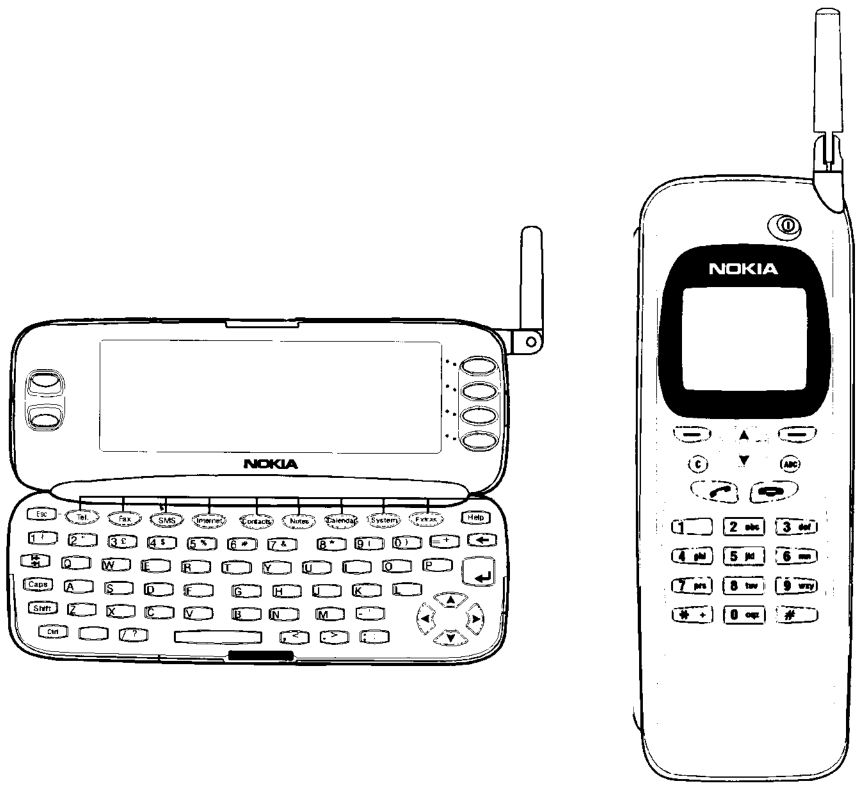

Figure 1. NOKIA 9000 Communicator

The phone interface looks and operates like other NOKIA cellular phones (except that the earpiece and microphone are located on the rear of the device). The phone interface is switched on and off by pressing the button on the cover.

The communicator interface has many organiser and communication applications and features a QWERTY keyboard, command buttons and large display for easy application use. The communicator interface has no power on/off button and is activated when the cover is opened and deactivated it is closed.

Communicator Applications

The application buttons on the communicator interface keyboard are used to start the corresponding applications.

Tel.— Telephone is used for managing voice calls.

Fax — Fax enables you to send any of your own documents as a fax. Faxes received can be read or forwarded.

SMS — Short Message Service enables you to send short messages. Short messages received can be read, forwarded or replied to.

Internet — Internet applications include Internet and modem–based applications: Mail, World Wide Web, Telnet and Terminal (VT100 compliant).

Contacts — Contacts is used for managing contact information: names, numbers and addresses.

Notes — Notes is used for text editing, printing and document management.
You can also send documents as SMS, fax or mail in the Notes application.

Calendar — Calendar contains an appointment book and a to–do list. You can set alarms and attach memos to events.

System — System contains desktop connectivity, security and other system related applications.

Extras — Extras applications include Calculator, Clock and Composer.

Help — Context sensitive help feature.

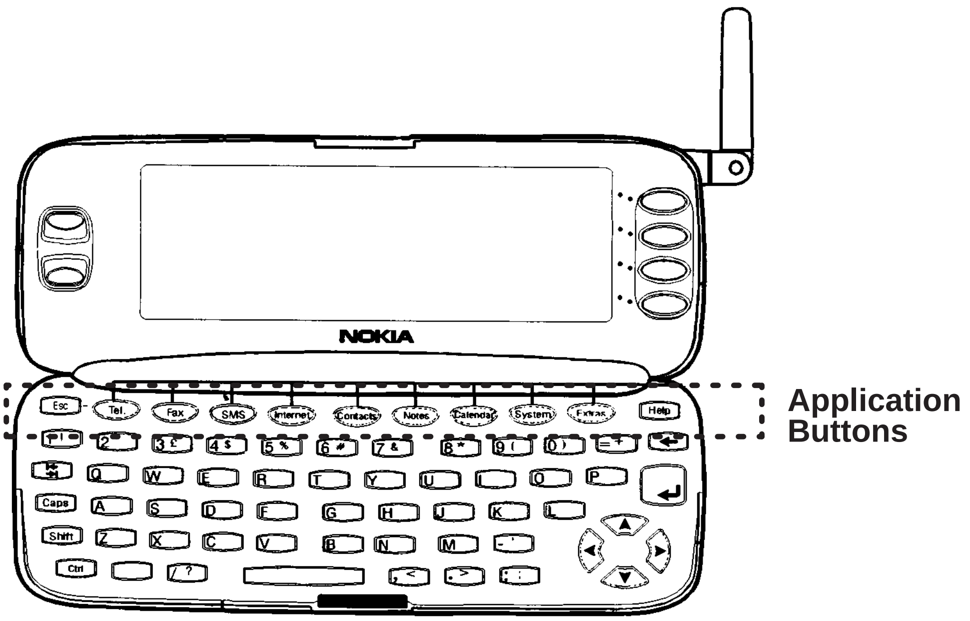

Figure 2. Communicator – Applications

CMT Operation

In order to make phone calls, the communicator must have a proper SIM card fitted and the phone interface must be switched on using the  button.

Note

- Opening or closing the cover does not affect active phone calls.
- The phone interface keys are not functional when the device cover is open.
- If you have an active phone call and you open the cover, the phone application will start automatically, and you can continue the call in the communicator interface.

Whenever you have made a voice call via the phone interface and change to the communicator interface, the audio is off (see “Audio Control”). When you make a call via the communicator interface (with the **Tel** application), the audio is on.

List Of Keys

When operating the phone interface, keys are pressed one at a time. Two keys are never to be pressed simultaneously.

	Switches the phone interface on and off. This button does not function when the device cover is open.
	This rocker key is used to scroll through menus, sub–menus or settings. If there are no active calls, the scroll keys can be used to browse through the memory contents. When a call is active, pressing scroll keys adjusts the volume level.
	Dials a phone number and answers a call.
	Ends an active call.
C	Deletes characters or exits the menu facility and memory functions.
ABC	Switches between alpha mode and numeric mode. In the menu facility, this key produces a help text on the current function.
0 to **9**	Number and alpha keys.
***** and #	Used for special purposes and certain functions.

Pressing **Menu** (the selection key under the text *Menu*) gains access to the menu functions and **Memory** (selection key under the text *Memory*) to the memory functions. The functions change according to the situation and previous selection.

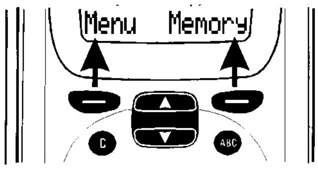

Figure 3. Selection Keys

Display Indicators

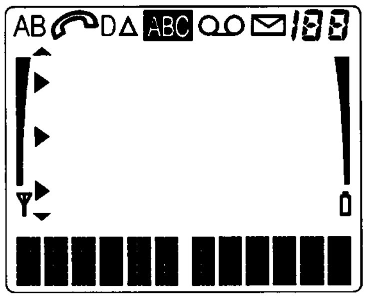

Figure 4. Display Indicators

AB Indicates which memory is currently selected. **“A”** refers to the SIM card memory and **“B”** to the communicator’s memory.

▶ Indicates that there is a list of options to select from.

Indicates that a voice call is in progress.

Indicates either: memory location, menu,submenu or setting option.

△ Roaming - when used in networks other than your subscribed one.

ABC The phone interface is in alpha mode.

and bar. Indicates that the current signal strength.

D A data or fax call is in progress.

Indicates an SMS message,fax or written mail has been received.

and bar. Indicates how much charge there is left in the battery.

Indicates an SMS message,fax or mail has been received.

Indicates a voice mail message has been received.

Getting Started

Switch on/off	Press and hold key.
Make a call	Key in the number (include area code if necessary). Press key.
Answer a call	Press or any other key except or * If you do not wish to answer the call, pressing will send out a busy tone to the caller.
End a call	Press key.
Clear digit	Press **C** key.
Clear display	Press and hold **C** key.
Last number redial	Press and the rocker keys, ▲ or ▼ to recall last number dialled.
Adjust audio volume	When in a call (or there is a call on hold) press ▲ or ▼ on the rocker key.
Activate keyguard	Press Menu soft key then press # within 3 seconds (the phone must be switched on). The display will show the message **Keypad Locked**, and respond with help text if any key is pressed.
De–activate keyguard	Press the Menu soft key and then ***** again. The display shows **Keypad activated.**
Calling the emergency services	Hold **C** key to clear display, ensure phone is in number entry mode. If in doubt press **ABC** . Enter emergency number. Press the key.

Using Memory

Phone numbers and names you store are normally located in the standard memory of the communicator, indicated by the letter “B” on the phone interface display.

The “B” memory is the communicator memory, the Contacts directory. When the communicator is started–up for the first time, the “B” memory is selected automatically.

The “A” memory is located on the SIM card that is inserted in the communicator. The SIM card memory uses numbered memory locations to store data. When numbers are saved in the SIM card (“A”) memory, a message will indicate its location number. The number of standard memory locations available on SIM cards varies from one card to another.

When the “A” memory is selected, the phone interface stores all contact information on the SIM card and cannot access the Contacts directory. Therefore, the use of the communications applications of the communicator interface will be less convenient (you will have to enter most contact information manually). This manual will assume that you use the standard “B” memory.

Storing information	Press **Memory**, Key in the name (of up to 30 characters) that you want to store with the phone number. Press **Save**.· Key in the international access and country codes (if necessary), area code and phone number. Press **Save**. The message SAVED will appear (in the middle of the display). The entry will be automatically saved in the Contacts directory in alphabetical order (numbers will precede letters).
Speed Dial /Search	*Speed Dial* – Key in the number of the memory /location of the stored phone number. Press or **Note:** Speed dialling is not possible during a call.
Recalling information	Press Memory, Key in the name or its first letter(s).· Press Find. The name closest to the keyed in characters will appear. You can move to the next name containing the same characters by pressing the scroll keys. *Speed Search*–Press Find. The first matching name appears with the cursor blinking under the last matching character you keyed in. If the found name was not the one you searched for, scroll to view the next matching name. When the name of the contact you want to call is shown on display, press Press ABC to view the associated phone number If the phone number has been designated a speed dial number, the location number of the name and phone number is shown in the upper right corner of the display.

Using the Menus

The phone interface offers a set of menu functions, which allow you to tailor the phone interface to your particular use. In each menu and submenu, you can check and alter the setting of any particular function. The menus and sub–menus can be entered by scrolling the menu or using appropriate menu shortcuts. Menu functions are accessible even during a call.

The following menu structure lists the names of the main menus and their sub–menus. Third–level menus are not shown here.

Some menu functions are shown in *italics*, these denote a network service.

Enter menu	Press **MENU** key.
Scroll	Press  to scroll thru menu options
Select function	Press **Select** to view sub–menu options and then **Select** again to modify the option.
Shortcut facility	Press **MENU** key, then enter the number of the menu function required (see following table).

The main menu features available are listed in the table below:

Menu No. / Shortcut	Main Menu	Sub–Menus
MENU 1	RECENT CALLS	1 Dialled calls 2 Received calls 3 Missed calls 4. Erase all recent Calls
MENU 2	MESSAGES	*1 Listen to voice messages* *2 Set voice mailbox number ,* *3 Read messages* *4 Broadcast messages*
MENU 3	VOICE CALL DIVERTING	*1 Divert all voice calls* *2 Divert when busy,* *3 Divert when not answered* *4 Divert if not reachable* *5 Cancel all diverts*

Menu No. / Shortcut	Main Menu	Sub–Menus
MENU 4	PHONE SETTINGS	1 Lights 2 Ringing volume 3 Ringing tone 4 Keypad tones 5 Warning tones 6 One touch dialling *7 Automatic answer* *8 Cell info display* *9 own number sending* 10 Call waiting 11 Restore factory settings 12 Menu list
MENU 5	SECURITY OPTIONS	1 PIN code request, 2 SIM change security 3 Voice Call barring 4 View fixed dial list 5 Fixed dialling 6 Change access codes 7 Closed user group 8 System lock
MENU 6	DURATION AND COST	1 Call duration *2 Call costs* 3 Call costs limit *4 Show costs in*
MENU 7	NETWORK SELECTION	
MENU 8	MEMORY FUNCTIONS	1 Memory selection 2 SIMcard memory status 3 Copy between memories 4 Erase SIMcard memory 5 Show own number
MENU 9	IN–CALL OPTIONS	
MENU 10	ALL SOUNDS	
MENU 11	KEYPAD LOCK	

PDA Operation

When the cover is opened, the application which was active last, appears in the same state. However, if you have made or answered a voice call in the phone interface and switch to the communicator interface by opening the device cover, the telephone application starts automatically.

To switch to another application, press the corresponding application button; you can do this even during an active call.

You need not "exit" any application before starting another as all inactive applications remain "frozen" until they are activated again. However, if the battery is removed or completely discharged, all data is saved but applications will return to their default states.

An auto save occurs every 5 minutes and when an application is changed, all data is saved automatically. Data is also saved when pressing the **Close** command button or closing the device cover.

Every time the cover is opened a note is shown listing any unread faxes, mail or short messages, unsent documents and missed calls.

Keys and Buttons

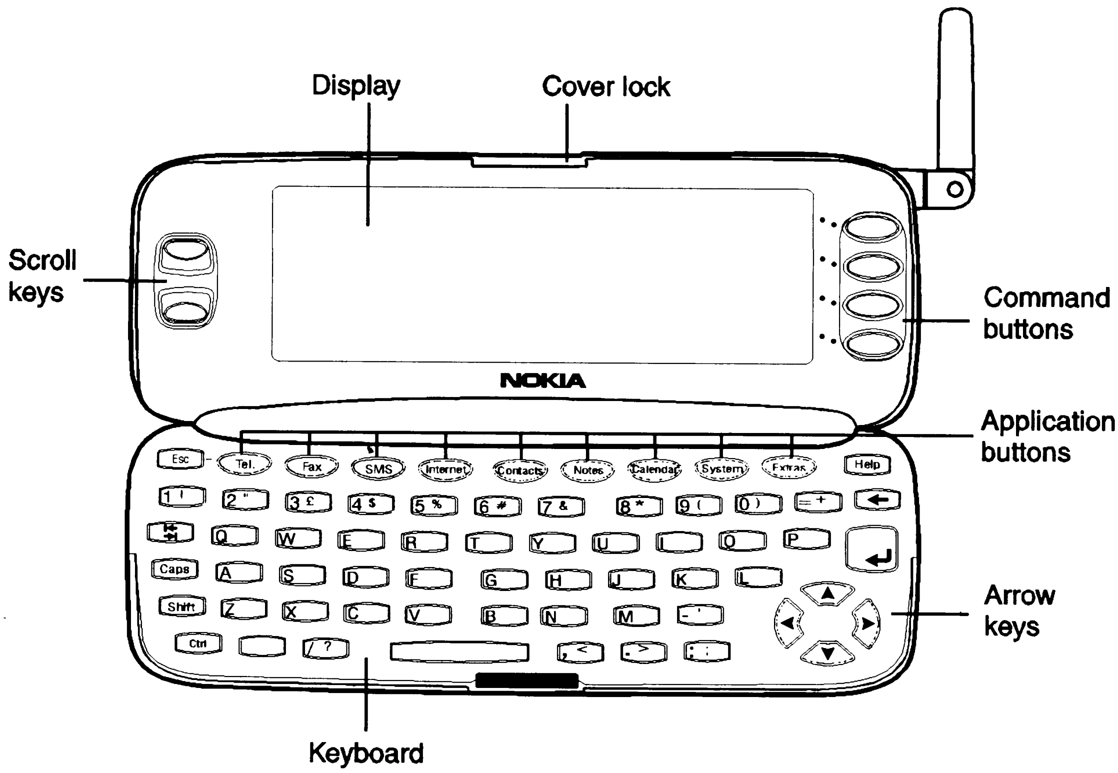

Figure 5. PDA Layout

Scroll Keys

Whenever the selection frame is shown, you can select items by moving the selection frame with the scroll buttons.

Arrow Keys

As above; some applications employ these keys for special functions.

Application buttons

The row of buttons at the top of the keyboard (starting from Tel.) activate the corresponding applications.

Keyboard Keys

ESC – cancels an action, as does the **Cancel** key. The ESC key can only be used when **Cancel** is among the available commands. All information notes shown on the display can also be dismissed with the ESC key (instead of pressing the **OK** command).

SHIFT – plus a letter key inserts an uppercase letter in front of the cursor. The SHIFT key does not need to be held down when pressing a key - once you have pressed the SHIFT key, the next key press always generates a shifted character.

CTRL – pressed together with certain keys, generates shortcut commands which can be used in most viewers and text editors.

CHR – Some of the numeric keys have a third character printed on them, pressing CHR and the key inserts the third character in front of the cursor. The CHR key also generates other special characters not shown on the keyboard, see “Notes: Editing” in the User Guide.

ENTER – When in a document or note – adds a new line
– When in the *Contact directory* – opens a contact card.

Pressing ENTER moves the cursor to the beginning of the next line or adds a new line. The ENTER key can also be used to select contacts and contact information in the Contacts directory. When information notes are shown, you may press ENTER instead of the **OK** command. In options and settings, when the value can be toggled, you may press ENTER instead of **Change.**Command Buttons

The commands always relate to the column of four command buttons on the right side of the display; these will vary according to the application selected.

HELP –Pressing the HELP button activates a context sensitive on–line help.

Audio Control

The audio control enables you to adjust the volume level and to activate the communicator’s handsfree operation.

To activate the handsfree operation, press the **Audio on** command button. After audio has been activated, the command changes to **Audio control**. Pressing **Audio control** lets you adjust the speaker volume or turn audio off. The indicator in the audio control view shows the chosen volume level.

Contacts

The *Contacts directory* is used by all communications applications: Telephone, Fax, SMS and the Mail applications. The *Contacts directory* lets you view and edit all contact information in the form of *Contact cards.*

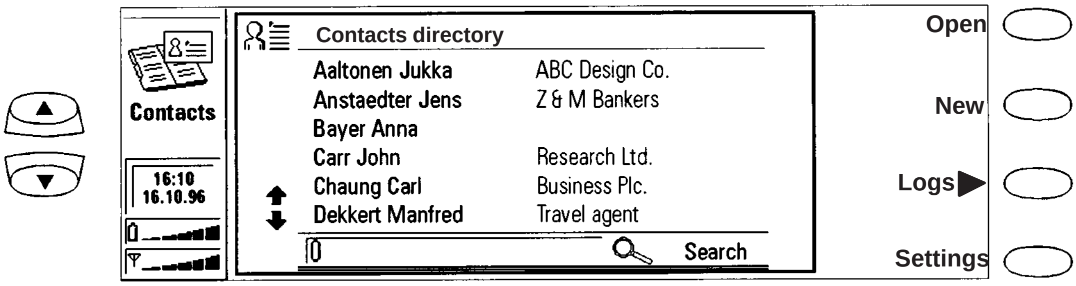

Figure 6. Contacts Directory

The main view shows the *Contacts directory.* This is a list of all *Contact cards* and are listed in alphabetical order according to the first name in each Contact card's 'Name' field.

To create a new *Contact card,* press **New** in the Contacts main view.

To open an existing *Contact card,* locate the card you want to open and press **Open.**

When the card you are searching for is shown, select it with the selection frame and press **Open.**

Contact Cards

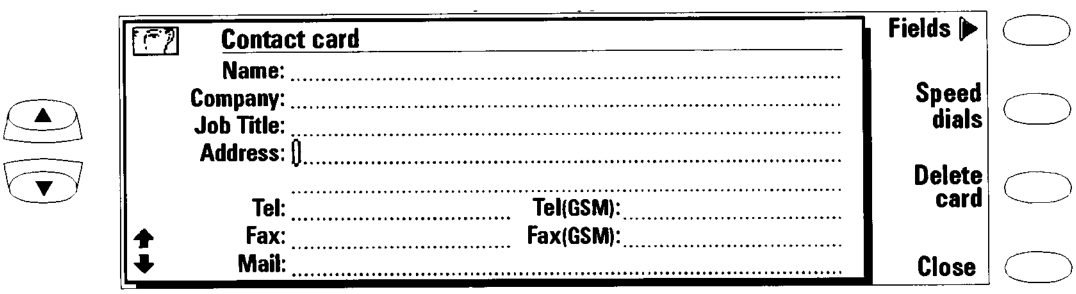

Figure 7. Contact Card

To edit or fill in a card use the keyboard and arrow keys. **Fields** is for adding extra fields or editing, modifying and deleting them. **Speed Dials** is for setting quick dialling to a contacts number. It is only functional from the Phone interface.

To delete a card, open it and press **Delete card**

Telephone

Tel is used for making and receiving voice calls and adjusting the Telephone settings.

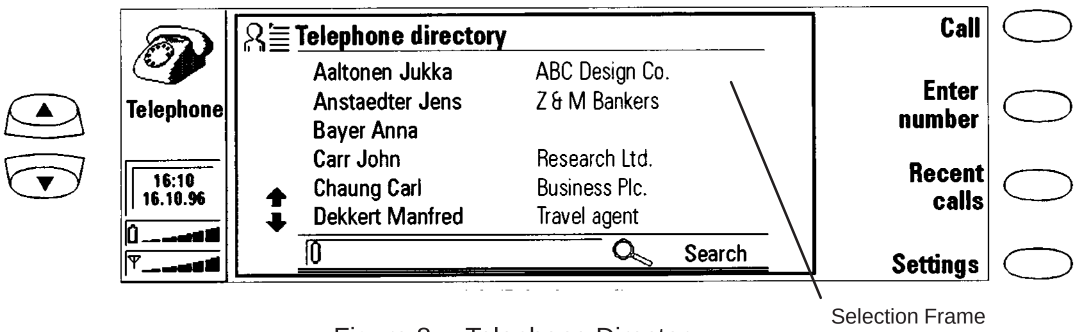

Figure 8. Telephone Directory

Making a Call From The Directory

Select the contact you want to call by moving the selection frame over the contacts name and press **Call** . If the contact has only one phone number, the number is called directly.

If the contact has more than one phone number, a pop–up box opens, listing the phone numbers. Choose the correct number from the list and press **Call .**

Making a Call Manually

Press **Enter number.**

Key in a phone number and press **Call.**

Answering Calls

You can answer a call either from the phone interface or from the communicator interface. To answer a call from the communicator interface:
Activate the Telephone application by pressing the *Tel.* application button.
Press **Answer.**

Note If you answer a call from the phone interface, but later choose to switch to the communicator interface, note that the audio is off (to turn audio on, press **Audio On**).

If you do not want to answer the call, press **End call.**

Fax

Faxes are received automatically, to activate, press the *Fax* button on the communicator interface keyboard. Fax sending and receiving is not possible if you already have an active voice or data call (the call indicator is shown in the indicator area).

The *Fax* main view shows two folders, ‘Own texts’ and ‘Received faxes’, and the ‘Document Outbox’ which acts as a storage folder (see User Guide for further information). The ‘Received faxes’ folder contains all received faxes and ‘Own texts’ includes all created faxes, short messages, memos, notes and user’s mail. Use scroll keys to select.

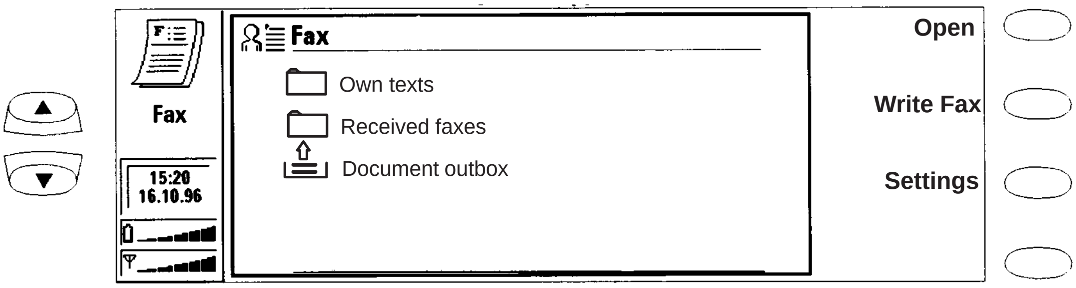

Figure 9. Fax Main View

Sending a New Fax

Press **Write fax.**

Input fax information at the cursor prompt. **Style** changes fonts and text sizes.

Press **Recipient,** the *Fax Directory* is displayed

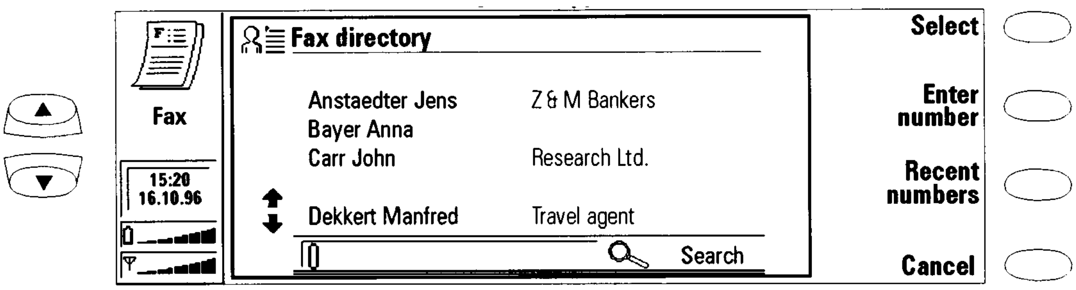

Figure 10. Fax Directory

To choose a recipient in the Fax directory, select a contact (by scrolling or searching). The names of contacts who have no fax number are dimmed and cannot be selected.

Press **Select.**

Check the info shown is correct and press **Send.**

Sending a Fax from Own Texts folder

To send your own text as fax:

Select the ‘Own texts’ folder in the Fax main view and press **Open**.

Select a document and press **Open**.

Press **Recipient** to access the Fax directory, select a contact.

Press **Select**

Check the info shown is correct and press **Send**

Sending from Received Faxes folder

To forward on a received fax :

Select the ‘Received faxes’ folder in the Fax main view and press **Open**.

Select a fax and press **Open**.

Press **Forward** to access the Fax directory, select a contact.

Press **Select**

Check the info shown is correct and press **Send**

Receiving Faxes

Faxes are received automatically. When a new fax has been received, you will hear a beep (unless the system is set to silent service mode) and an information note is shown on the screen. Received faxes go automatically in the ‘Received faxes’ folder. Unread received faxes are marked with an icon.

To rename or delete the selected fax, open the ‘Received faxes’ folder and press **Rename** or **Delete**

To view a received fax, open the ‘Received faxes’ folder, select a fax and press **Open**; the fax viewer opens . Use the scroll or the arrow keys to scroll the fax up, down or horizontally.

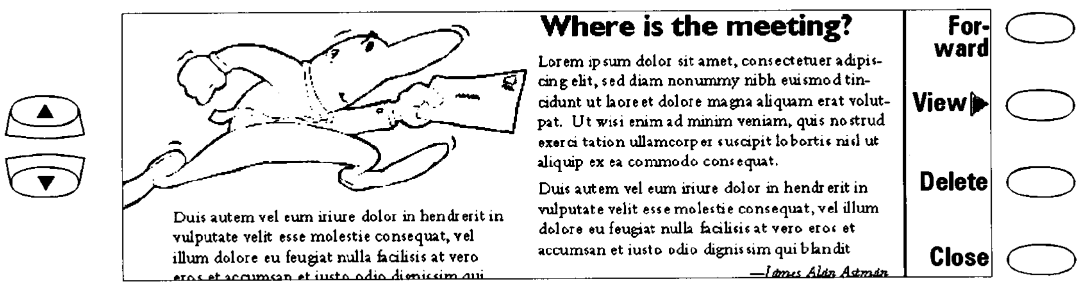

Figure 11. Fax Viewer

Pressing **View** allows **Zoom in / Zoom out** functions to be performed.

Rotate rotates the fax 90 degrees clockwise with each key press

Delete deletes the viewed fax.

SMS (Short Message Service)

Tel | Fax | SMS | Internet | Contacts | Notes | Calendar | System | Extras

The Short Message Service (SMS) is a network service and enables you to send and receive short alphanumeric text messages of up to 160 characters over the digital cellular network.

Short messages are particularly well suited for sending short, urgent messages from one cellular phone to another: Sending is practically instantaneous, messages can be sent or received even during a voice or data call and can be read in any cellular phone that has the capability.

The *SMS* main view shows four folders and the ‘Document outbox’. The ‘Own texts’ folder contains texts that you have written, ‘Received messages’ contains short messages you have received, ‘Standard messages’ contains predefined message templates and ‘Business cards’ contains all Contact cards in the *Contacts directory.*

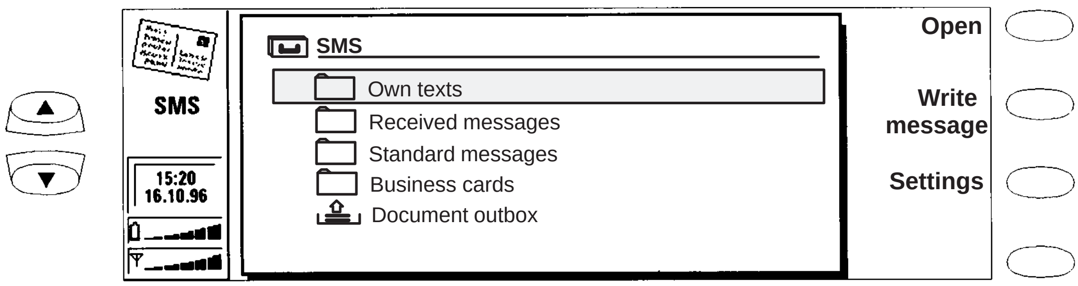

Figure 12. SMS Main View

Sending messages

To create a new short message:

Press **Write message** in the main view to open the SMS editor and write message.

When the message is ready to be sent press **Recipient**, select and send to the desired contact.

To send a previously created document:

Select the ‘Own texts’, ‘Standard messages’ or ‘Business cards’ folder and press **Open**.

Select a document and press **Open.** Only texts no longer than 160 characters can be opened.

When the message is ready to be sent press **Recipient**, select and send to the desired contact.

Receiving messages

When a new short message has arrived, a beep will sound (unless the system is set to silent service mode) and an information note is shown on the display. The note appears even if the SMS application is not active.

Received short messages go automatically in the ‘Received messages’ folder. A received short message can be a normal short message, business card, service card or notification of a voice message in your voice mailbox.

Unread received messages are marked with a postcard icon.

To read new short messages, start the SMS application (if it is not already active), open the ‘Received messages’ folder, select a message and press **Open**.

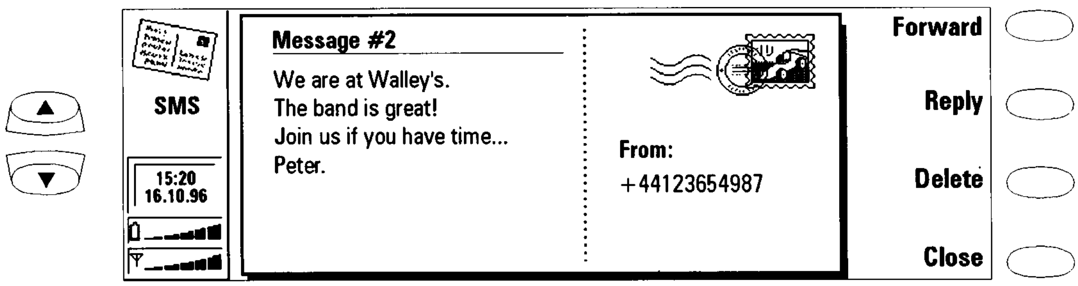

Figure 13. SMS Message received

Internet

Tel Fax SMS **Internet** Contacts Notes Calendar System Extras

Before you can connect to the Internet, you must open an account with an Internet access provider (see “Internet Settings” In the User Guide).

The Internet applications are:

Mail — An electronic text mail application which lets you send and receive text messages all over the world using the Internet network.

World Wide Web (WWW) — A hypertext–based system for finding and accessing resources on the Internet network.

Telnet — Allows connection to computers which provide terminal services through the Internet network.

Terminal — Allows connection to computers, like mainframe computers, which provide direct dial–in terminal services. Both Telnet and Terminal applications emulate the VT100 terminal.

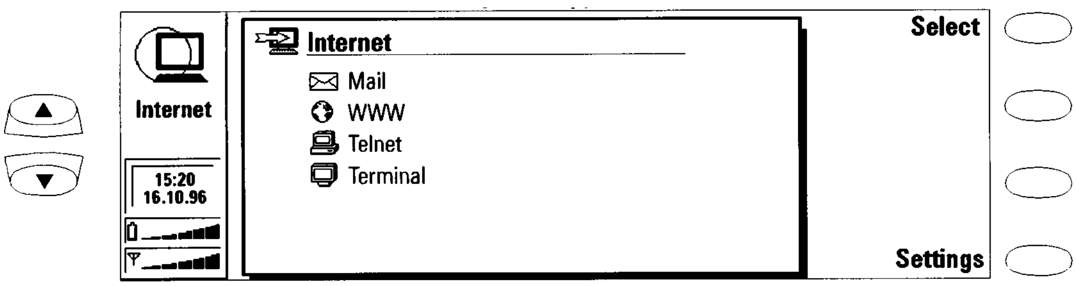

Figure 14. Internet main View

The Internet applications are started by selecting an application in the Internet main view and pressing **Select**. (If an Internet application is already active, you must close it by pressing **Close,** before you can start another).

Note: Depending on the network configuration and load, establishing an Internet connection may take some time.

If a connection is idle for longer than the factory set time–out period, the connection is terminated automatically. This time–out period applies to connections made with all Internet applications. In addition, the World Wide Web application has its own Auto disconnect period.

When you want to disconnect from the host, press **Hang up**. Disconnecting is indicated by a note and the data call indicator disappears. When the Internet applications main view returns on display, the communicator is no longer connected to the Internet.

Mail

Mail enables you to send and receive mail. The Mail system is compliant with the Internet standards SMTP, IMAP4 and MIME1.
'Own texts' – contains previously created texts.
'Received mail' – contains mail 'fetched' from the 'Remote mailbox.'
'Remote mailbox' – this is a network service and receives all incoming mail using the IMAP4 standard.
'Document outbox' – storage area for outgoing mail.

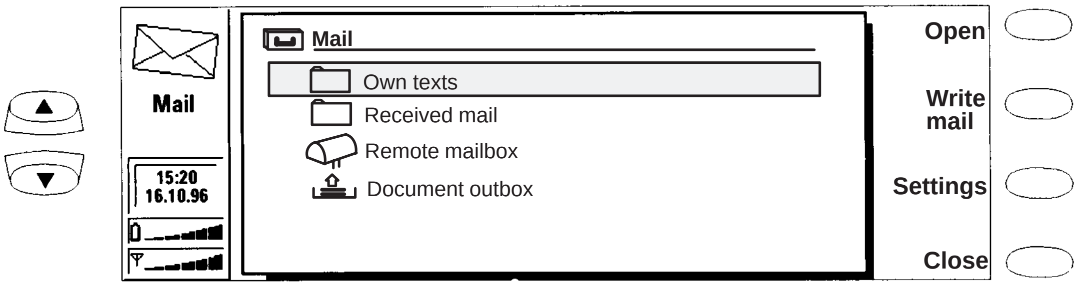

Figure 15. Mail – main view

Sending Mail
Press **Write mail.**
Write the contents of the mail message.
Press **Recipient,** the Mail directory view opens, select a contact or press **Enter address** to open the Mail envelope.

Figure 16. Mail – envelope

In the Mail envelope you can check the sending information and add more recipients (press **Add recipient** or enter addresses manually).
Press **Send** to send the message.

Reading Mail
In the Mail main view screen, move the selection frame over the 'Remote mailbox' folder and press **Connect**; All mail is listed and unread messages have unopened envelope icons attached to them.
You can get all new mail by selecting a message and pressing **Fetch selected.** Fetched mail goes to the 'Received mail' folder where it can be opened and read. Pressing **Fetch new** puts all new mail to the 'Received mail' folder.

World Wide Web

The World Wide Web application allows your communicator to become an internet browser and access Internet sites via hypertext–links (see the User Guide for information on setting up these links.)

Hotlist
The hotlist is where your pe–defined links to the WWW pages are stored; these are retrieved by pressing **Fetch**. If the WWW page has been recently downloaded, the page is retrieved from memory, if not, the page is downloaded from the Internet by making a GSM data call to your Internet Access Point.

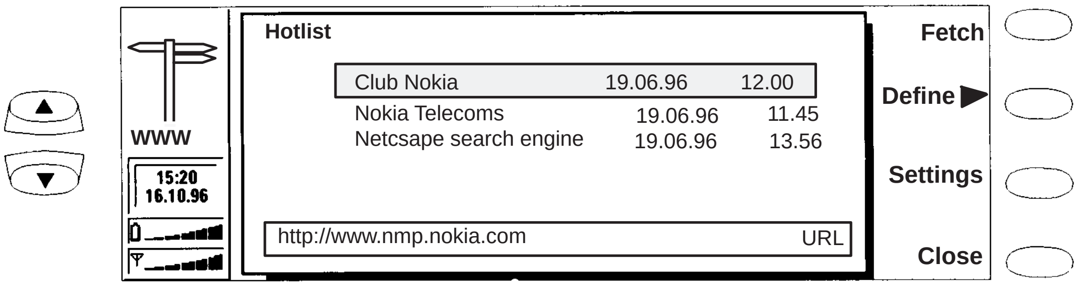

Figure 17. WWW – Hotlist

The World Wide Web facilities on the communicator are quite extensive, see the User Guide for full explanations.

Telnet and Terminal

Allows connection to mainframe computers providing terminal services through the Internet; both applications emulate the VT100 terminal display. Once a connection is established a login name and password are normally required in order to be able to use the services provided by the host computer.

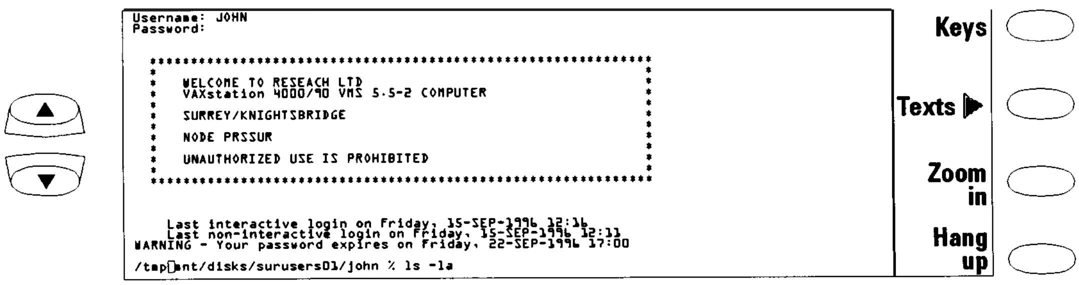

Figure 18. Telnet –VT100 emulation

Press **Connect** in the Terminal connections screen

Press **Hang up** to disconnect.

Notes

Notes is used for writing notes and managing various documents stored on the communicator. All folders, and the ‘Document outbox’, are shown in the *Notes* main view.

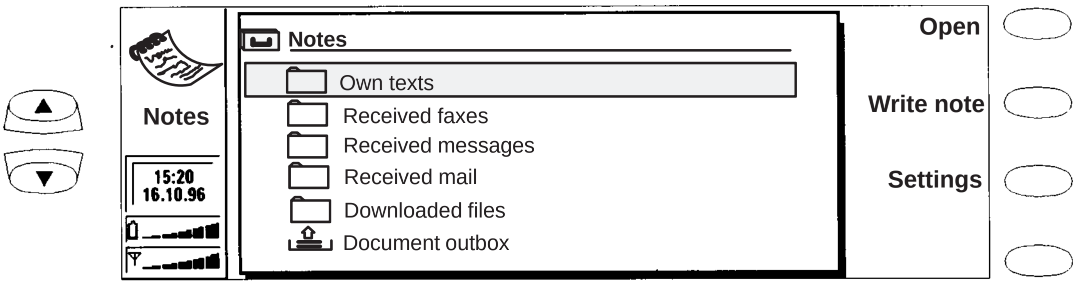

Figure 19. Notes – main view

Reading Documents

Select a folder and press **Open**.

Select a document from the folder’s document list and press **Open**.

Creating Documents

Press **Write note** in the Notes main view. A new document is created in the ‘Own texts’ folder.

Enter text in the note editor.

Deleting Documents

Select a folder and press **Open**.

Select a document from the folder’s document list and press **Delete**.

Sending Documents

From the editor, Press **Print/Send**, a pop–up box listing printing and sending options opens, these are:–

Print

Send as a fax,

Send as short message

Send as mail

Select contact from the corresponding directory and send.

Calendar

Tel Fax SMS Internet Contacts Notes **Calendar** System Extras

The Calendar has two views; the Month view shows a month at a time, and the Day view shows the calendar events of a day. The Calendar is also used to link memos to events and also incorporates a daily *To–do list.*

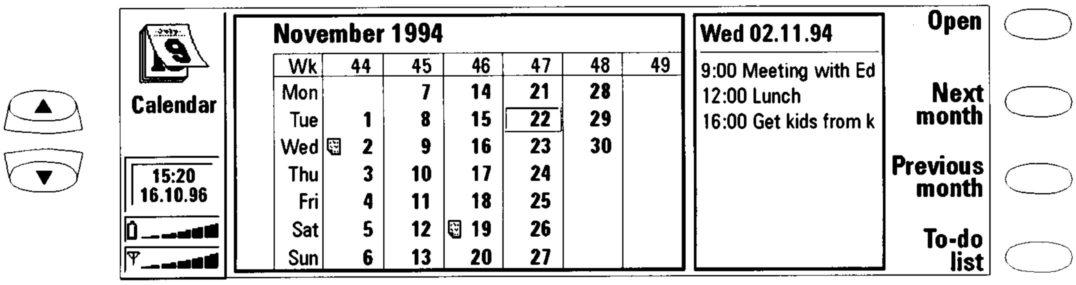

Figure 20. Calendar – main view

Month View

The Month view shows the days of the current month in columns according to the number of the week (on the top row).

In the Month view, days that have scheduled events are indicated by an icon (Nov 2 and 19 in the figure above). If the selected day contains scheduled events they are shown in a separate daily events list on the right side of the display.

The schedule can be edited in the *Day view* – press **Open**.

To view next months appointments – press **Next month.**

To view the previous months appointments – press **Previous month.**

To write yourself reminders of important matters, press **To–do list**.

Day View

Day view displays the events of the selected day. The first event of the day is always shown when the list opens; event entries are freely editable.

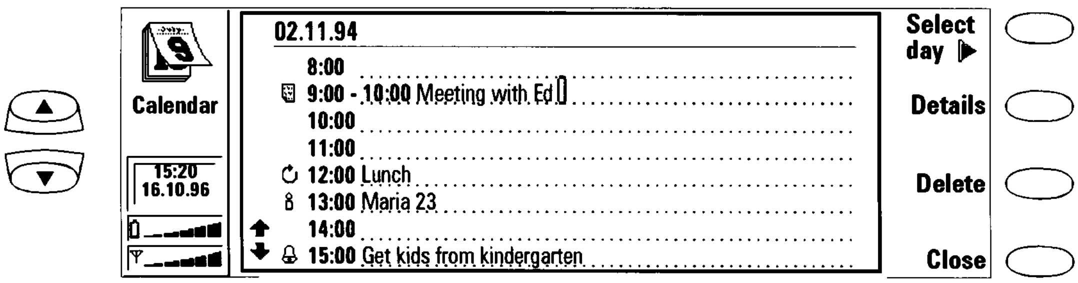

Figure 21. Calendar – day view

Figure 21 shows an example of a day view page with icons attached to various entries. These are as follows:–

Attached memo

Alarm

Repeating event (daily, weekly, monthly)

Annual event

To add events, move the selection frame over the starting time of the event and enter on the dotted line.

To delete events, select the event and press **Delete**. If you delete (or edit) repeating events, you will be asked if you want to apply the changes to all or only to the current event.

To–do List

The To–do list is accessed by pressing the **To–do list** command button in the Month view. The To–do list is a list of tasks not connected to any specific time or day.

After a calendar alarm has occurred, you have the opportunity to move the message contents of the alarm to the To–do list by pressing **Move to To–do list** command button.

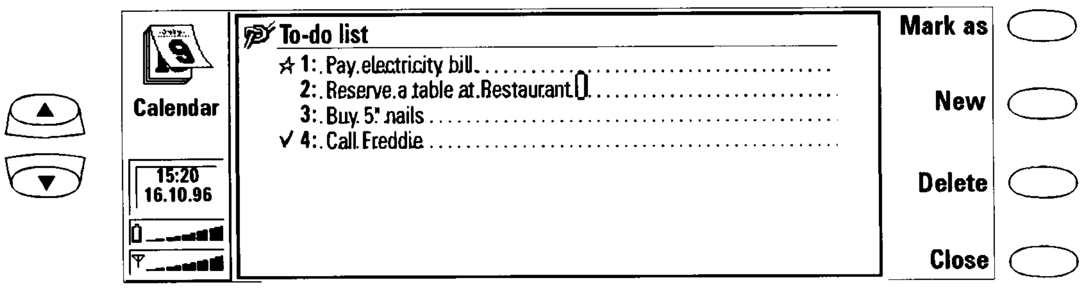

Figure 22. Calendar – to do list

The entries in the To–do list are numbered, and can be given high priority (denoted by a star icon) or ticked as completed. High priority entries are always shown at the top of the list.

System

The main view shows a list of applications that can be launched; scroll to an application and press **Select.**

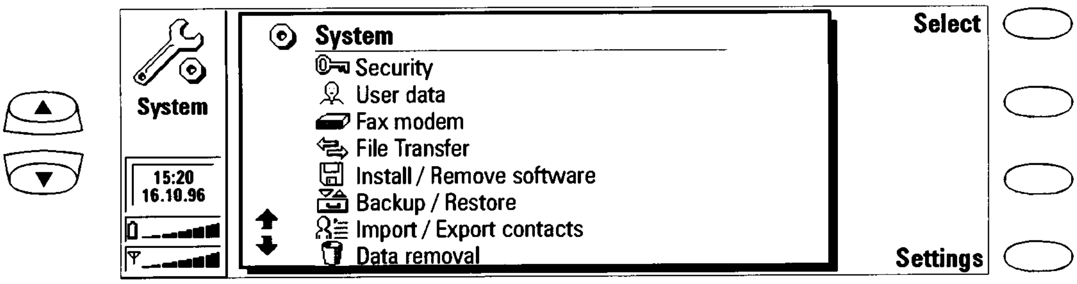

Figure 23. System – main view

The following applications require connection to a PC and the supplied **Nokia connect** programme to be running.
File transfer
Install / Remove software
Backup / Restore
Import / Export contacts

The software requires Microsoft Windows 3.1 or later and requires connection to an available serial or infrared (IrDA compatible) port.

Security

Press **Select** and then **Settings** to define the locking codes, passwords etc. If the time–out locking feature has already been activated the **Lock System** command in the Security main view will lock the communicator immediately.

User Data

This shows your own *contact* sheet which is used in fax cover pages.

Fax Modem

The communicator can function as a normal 9600 bps fax–modem and be utilised by any stand alone PC. To change the communicator to a fax–modem, press **Activate.** Press **Disable** to disconnect the mode.

You can connect the communicator to a PC either by infrared or cable connection (PC connectivity software not needed). Press **Settings** and then **Change.**

When the communicator is used as a fax–modem, other communication features are disabled but the communicator interface remains functional.

File Transfer

To connect to a PC, press **Connect to PC**
The right window shows the directories of the PC, the left window shows the communicator folders. In order to transfer the selected file, you must first open the directory or folder you are transferring files to.

Installing / Removing Software

This allows installation or removal of new and update existing communicator applications, drivers and other system software components.

Backup / Restore

This allows data backups and the facility to restore it later. The *Backup/Restore* main view shows the data group which will be backed up or restored, current connection type and the current PC directory.

Importing / Exporting Contacts

Contact information can be exported or imported as an ASCII file which can then be edited on a PC. When *Import/Export contacts,* is selected, the System main view displays the connection type used and the default path in the PC.

Data Removal

This enables data to be deleted from the communicator. The data is arranged into four groups: All data, Calendar data, Documents plus Contacts and Speed dials.

Settings

Changes can be made to the following communicator settings:–

Contrast control –

Screen blanker period –

System sounds –

Preferences –

Scroll to required setting and press **Change**; options are self–explanatory.

Extras

The Extras application group contains:–
Calculator
Clock
Composer
Future communicator add–on software will also be installed in the Extras application group.

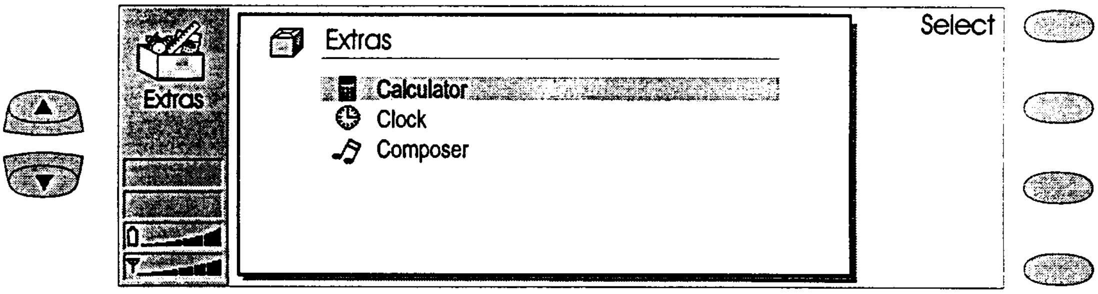

Figure 24. Extras –main view

To start one of the applications, scroll to an application and press **Select**. If one Extras application is active, you must close it by pressing **Close** before you can start another.

Calculator

The calculation is entered from the keyboard into the entry field at the bottom of the screen. Press **Enter** to perform the calculation; previous calculations are shown in the list above the entry field. The list can be scrolled with the scroll keys and cleared by pressing **Clear list.**

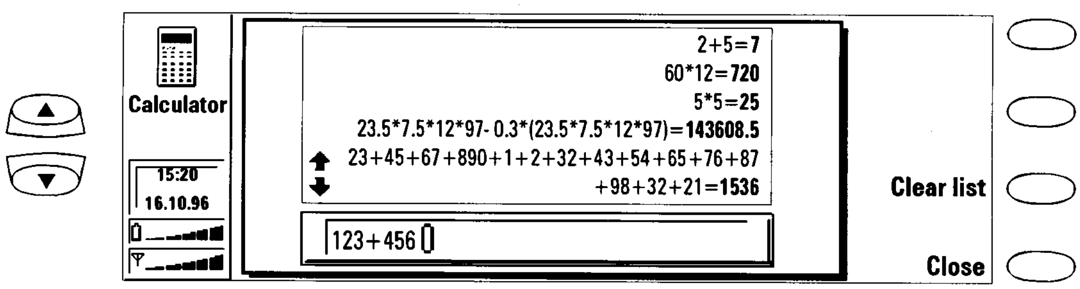

Figure 25. Extras –calculator

Clock

The Clock shows the time and date in your home city and country, as well as in several other cities and countries throughout the world. The Clock also includes an alarm clock. The system time and date can be adjusted in the Clock settings.

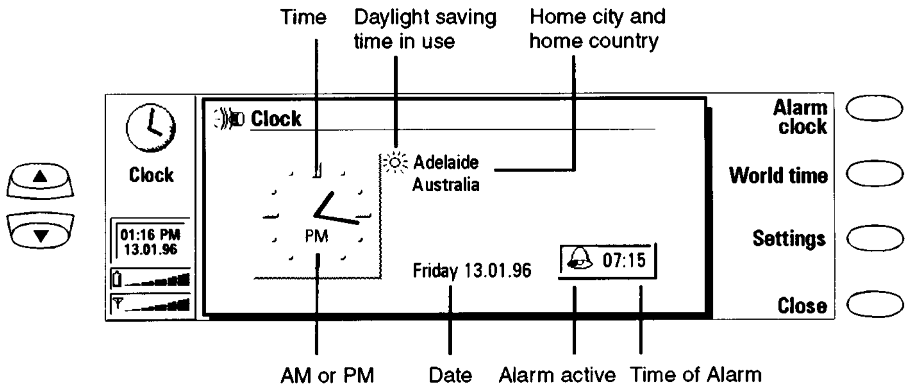

Figure 26. Extras –clock main view

Alarm Clock –
The Alarm clock is activated with the **Alarm clock** command in the Clock main view. The counter below the alarm clock is shown only if there is an active alarm and this activates according to the home city time.

World Time –
World time is activated with the **World time** command in the Clock main view. The world map shows the currently elected destination city on the world map in cross hairs.

The Home box shows information on the currently selected home city.

The Destination box shows the same information for the currently selected destination city, as well as the international call prefixes needed to make a call from the home city to the destination city.

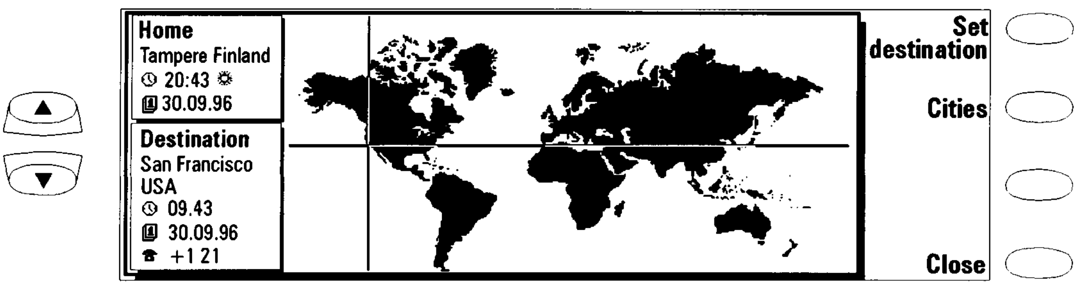

Figure 27. Extras –clock world time

Composer

The Composer application enables you to compose customised phone ringing tones. The Composer can be started from both the Telephone application and from the Extras application group. The main view lists all available ringing tones, but you can edit the three custom tones.

Figure 28. Extras –composer

Help

Help is context –sensitive and if pressed will always display a help file about the application you are in. Pressing **Application topics** gives you a list of topics covered for that application.

To view a list of general help topics, including a troubleshooting guide, press **General topics**

To return to the active application, press **Close.**

Document Outbox

All documents you send go through the Document outbox where they are sent automatically whenever it is possible to do so. The Document outbox can be accessed in the *Fax, SMS, Mail* and *Notes* applications main views, where it is shown at the bottom of the folders list. To open the Document outbox, select the *Document outbox* from the list and press **Open.** Press **Start** to send a document; the top of the list is sent first,

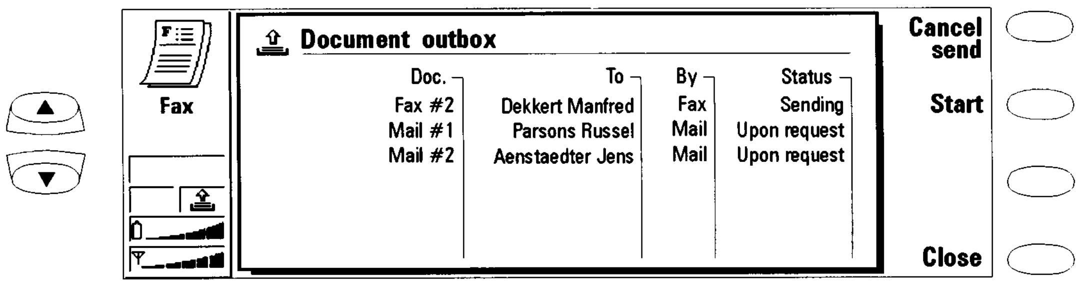

Figure 29. Document outbox

NOTES